DINAMAP™ *PLUS*
Vital Signs Monitor

Service Manual

CRITIKON

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PRELIMINARY

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CRITIKON, INC. ❑ 4110 George Road ❑ Tampa, Florida U.S.A. 33634 ❑ (813)887-2000 ❑ Telex 494 3183

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TABLE OF CONTENTS

SECTION 1. INTRODUCTION	1.1	Scope of Manual	1-1
	1.2	Manual Changes	1-2
	1.3	Service Policy	1-2
	1.3.1	Technical Assistance	1-3
	1.3.1.1	Via Phone	1-3
	1.3.1.2	Via FAX	1-4
	1.3.2	Repair Service	1-4
	1.3.3	Repair Parts	1-5
	1.4	Product Description	1-5
	1.4.1	General Description	1-5
	1.4.2	Physical Description	1-6
	1.4.3	Storage Batteries	1-6
	1.4.4	Product Reorder Information	1-8
	1.4.5	Accessory Reorder Information	1-8
	1.4.5.1	Critikon Accessories	1-8
	1.4.5.2	After-Market Accessories	1-10
	1.4.6	Specifications	1-10
SECTION 2. THEORY OF OPERATION	2.1	Introduction	2-1
	2.2	System Theory of Operation	2-1
	2.3	Functional Theory of Operation	2-3
	2.3.1	System Processor	2-3
	2.3.2	Data Acquisition System	2-4
	2.3.3	Pulse Oximetry System	2-6
	2.3.4	NIBP System	2-7
	2.3.5	Pneumatics System	2-8
	2.3.6	Power Supply	2-10
	2.4	Schematic Descriptions	2-13
	2.4.1	System Processor Board	2-13
	2.4.1.1	Failsafe Logic	2-15
	2.4.1.2	Read-Only Memory	2-16
	2.4.1.3	Read/Write Memory	2-17
	2.4.1.4	Serial EEPROM	2-17
	2.4.1.5	Analog Input Subsystem	2-18
	2.4.1.6	Graphics Subsystem	2-19
	2.4.1.7	Realtime Clock	2-20
	2.4.1.8	Audio Subsystem	2-20
	2.4.1.9	Keypad Interface	2-22
	2.4.1.10	Digital Inputs	2-22
	2.4.1.11	Digital Output Ports	2-22

TABLE OF CONTENTS
CONTINUED

SECTION 2. THEORY OF OPERATION Continued	2.4.2	DAS Board	2-23
	2.4.2.1	DAS CPU, Opto-isolators, and Control Logic	2-24
	2.4.2.2	Analog To Digital Converter and Multiplexer	2-25
	2.4.2.3	ECG Channel and Lead Switching	2-26
	2.4.2.4	Invasive Pressure Channels	2-28
	2.4.2.5	Temperature Channel	2-29
	2.4.2.6	Isolated Power Supply	2-30
	2.4.2.7	Addressing	2-31
	2.4.2.8	Port Assignments	2-32
	2.4.2.9	A/D Converter	2-35
	2.4.3	Analog Board	2-35
	2.4.3.1	Control Interface and DAC	2-36
	2.4.3.2	Clock Generator and Sync	2-36
	2.4.3.3	Negative 12 Volt Power Supply	2-38
	2.4.3.4	Isolated Power Supply	2-39
	2.4.3.5	LED Current Control	2-40
	2.4.3.6	Sensor Code Detection	2-41
	2.4.3.7	Sensor AC Amplifiers	2-42
	2.4.3.8	Synchronous Detectors and Filters	2-43
	2.4.3.9	PO Pulse Amplifiers	2-43
	2.4.3.10	Pressure Transducer Excitation	2-44
	2.4.3.11	Transducer Amplifier	2-44
	2.4.3.12	BP Pulse Amplifier and Clamp	2-45
	2.4.4	Pneumatics Board	2-45
	2.4.4.1	Valve Drive Circuit	2-45
	2.4.4.2	Pump Drive Circuit	2-46
	2.4.4.3	Overpressure Switch and Safety Interlocks	2-46
	2.4.4.4	Time Delay Circuit	2-47
	2.4.4.5	Thermal Switch Circuit	2-48

TABLE OF CONTENTS
CONTINUED

SECTION 2. THEORY OF OPERATION Continued	2.4.5	Battery Switch Board	2-48
	2.4.5.1	Battery Switch Power Supply	2-49
	2.4.5.2	Battery to DC Source Switch	2-50
	2.4.5.3	Battery to Test Load Switch	2-50
	2.4.5.4	External Power Sources	2-51
	2.4.5.5	18V Bus Detector	2-51
	2.4.5.6	Power Supply Control Latch	2-52
	2.4.5.7	Battery Charger Controller	2-52
	2.4.5.8	Connector Signal Description	2-54
	2.4.6	Power Supply Board	2-55
	2.4.6.1	Low Voltage Converter	2-56
	2.4.6.2	Line Power Converter	2-57
	2.4.6.3	Battery Charger	2-59
	2.4.6.4	Control Logic	2-60
	2.4.7	Motherboard	2-61
SECTION 3. MAINTENANCE	3.1	Introduction	3-1
	3.2	Changing Fuses	3-1
	3.2.1	Line Power Fuse Replacement	3-1
	3.2.2	Battery Fuse Replacement	3-3
	3.3	Replacement of Backup Battery	3-4
	3.4	Service Mode Operation	3-4
	3.4.1	NIBP Tests	3-6
	3.4.1.1	Automatic Leak Test	3-7
	3.4.1.2	Pump Overpressure Test	3-8
	3.4.1.3	Valves Test	3-9
	3.4.1.4	Calibration Check	3-10
	3.4.2	IBP Tests	3-11
	3.4.3	Temperature Tests	3-13
	3.4.4	SpO2 Test	3-14
	3.4.5	More Tests	3-15
	3.4.6	Service Mode Exit	3-16

TABLE OF CONTENTS
CONTINUED

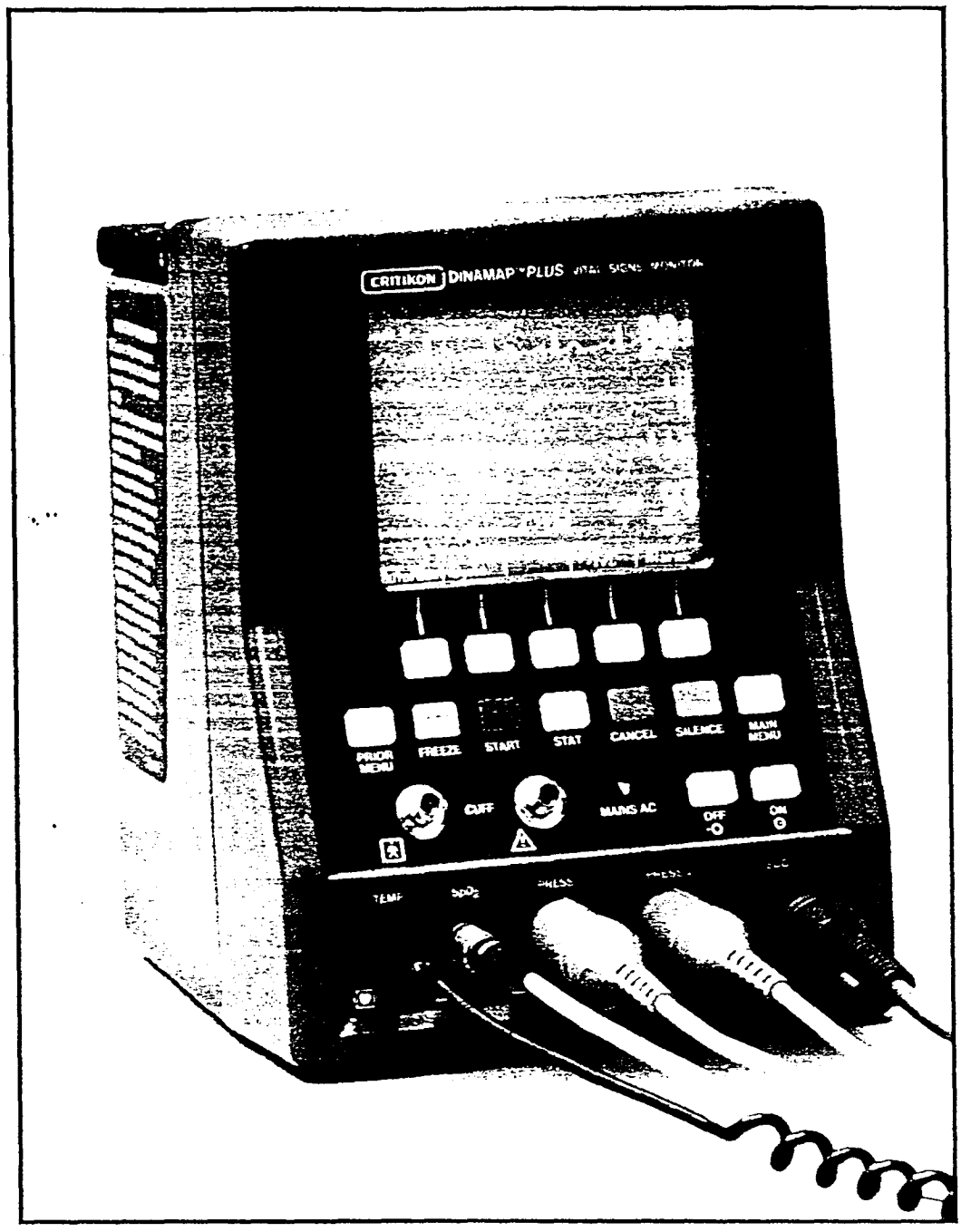
SECTION 3. MAINTENANCE Continued	3.5	Periodic Maintenance	3-17
	3.5.1	As Required	3-17
	3.5.1.1	Integrity of Hoses and Cuffs	3-17
	3.5.1.2	Cleaning of Monitor	3-17
	3.5.1.3	Cleaning of Accessories	3-17
	3.5.1.4	Storage of Monitor	3-19
	3.5.2	Annual Procedures	3-19
	3.6	NIBP Leak Test	3-19
	3.7	NIBP Calibration	3-21
	3.8	Alignment and Adjustment	3-25
	3.8.1	Five Volt Logic Power Supply	3-25
	3.8.2	Battery Charger Float Voltage	3-26
	3.8.3	Twelve Volt Analog Power Supply	3-26
	3.8.4	Pneumatics System Pressure Switch	3-27
	3.8.5	Pulse Oximeter Tuned Transformers	3-27
	3.9	Jumper Options	3-27
	3.10	Alarm Code Interpretation	3-27
	3.11	Care of Storage Batteries	3-31
	3.12	Ground Resistance Test	3-33
	3.13	Disassembly Procedures	3-34
	3.14	Reassembly Procedures	3-35
SECTION 4. SERVICE DIAGRAMS AND PARTS LISTS	4.1	Introduction	4-1
	4.2	List of Applicable Service Diagrams	4-1

LIST OF ILLUSTRATIONS

2-1	Model 8720 System Block Diagram	2-2
2-2	Pneumatics System Simplified Schematic	2-8
2-3	Power Distribution Diagram	2-12
FO-1	System Processor Block Diagram	2-63/64
FO-2	Data Acquisition System Block Diagram	2-65/66
FO-3	Pulse Oximetry System Block Diagram	2-67/68
FO-4	Non-Invasive Blood Pressure System Block Diagram	2-69/70
FO-5	Pneumatics System Block Diagram	2-71/72
FO-6	Power Supply Block Diagram	2-73/74
3-1	Pressure Calibration Check Setup	3-11
3-2	Cuff and Hose Leak Test Setup	3-20
3-3	Model 8720 Interconnection Diagram	3-37
3-4	Pneumatic Tubing Installation	3-39
4-1	Top Assembly	4-5/6
4-2	Sub-Top Assembly	4-7/8

LIST OF TABLES

1-1	Critikon Accessories	1-10
1-2	Mechanical Specifications	1-11
1-3	Environmental Specifications	1-11
1-4	Electrical Specifications	1-12
1-5	NIBP Performance Specifications	1-12
1-6	ECG Performance Specifications	1-14
1-7	SpO2 Performance Specifications	1-15
1-8	IBP Performance Specifications	1-16
1-9	Temperature Performance Specifications	1-17
1-10	Alarm Functions	1-17
3-1	System Error Alarms	3-28



DINAMAP™ *PLUS* Vital Signs Monitor, Model 8720

SECTION 1. INTRODUCTION

1.1 SCOPE OF MANUAL

This manual is intended for use by trained service technicians who are familiar with electromechanical devices and digital and analog circuit techniques. This Service Manual provides service and parts repair information for the DINAMAP™ *PLUS* Model 8720 Vital Signs Monitor.

WARNING

To reduce the risk of electric shock, do not remove cover or back. Refer servicing to qualified service personnel.

All unit repairs should be performed only by trained service technicians.

Voltages dangerous to life exist in this unit. Take care when servicing power supply and display assembly.

When troubleshooting power supply board, use an isolation transformer to isolate unit from ac line power. Use a variac and increase ac power input gradually while checking internal power circuit voltages.

For information about operating the Monitor in a clinical environment, refer to the separate Operation Manual.

The Service Manual consists of four sections:

- Section 1 describes this volume and tells you how to use it. Information is provided about the physical and functional characteristics of the Monitor. Information is also provided about getting assistance in the event the unit fails to function properly.

- Section 2 presents theory of operation for the overall monitor, then provides descriptions of each of the main functions of the Monitor. Schematic diagrams of each major assembly are also described in detail as a further aid in understanding circuit functions.

- Section 3 provides information about periodic and corrective maintenance of the Monitor. Procedures are included for performance tests, calibration, pneumatic leak tests, cuff and hose leak tests, and alignment and adjustment. Corrective maintenance information is provided for isolating faults to the module/subassembly level.

- Section 4 contains Illustrated Parts Breakdown (IPB) drawings, service diagrams, and related parts lists.

1.2 MANUAL CHANGES

If, in the normal use of this manual, you notice errors, omissions, or incorrect data, or if you can suggest comments that may help improve this manual, please complete the Publications Change Request form in the back of this manual. Submit the form to:

Critikon, Inc.
Marketing Services
P.O. Box 31800
4110 George Road
Tampa, Florida 33631-3800

Changes to the Service Manual, either in response to user input or to reflect continuing product improvements, are accomplished through reissue.

Changes occurring between reissues are addressed through Change Information Sheets and replacement pages. If a Change Information Sheet does not accompany your manual, the manual is correct as printed.

1.3 SERVICE POLICY

All repairs on products under warranty must be performed by Critikon personnel. Unauthorized repairs will void the warranty. Products out of warranty should be repaired by Critikon or a Critikon authorized affiliate repair facility.

1.3.1 Technical Assistance

If the product fails to function properly or requires maintenance and technical assistance is required, contact Critikon Technical Support.

Before contacting Technical Support:

- Have you checked the maintenance section of the Service Manual?
- Can you duplicate the problem? Please try to repeat the steps that initially caused the problem to appear.
- Make sure your accessories are not the cause of the problem. Many repairs can be avoided by checking all the accessories associated with the product.

If you are unable to resolve the problem after checking these items, please contact a Technical Support Specialist in one of the following ways:

1.3.1.1 Via Phone

- Call Critikon Technical Support Monday through Friday, 8:30 AM to 5:00 PM, Eastern Time at 1-800-237-5591.
- Please tell the person answering your call that you need Technical Support.
- We are interesting in providing all our customers the assistance they need, and we will take the time to answer all of your questions. When calling, please be prepared to wait a short time while we offer assistance to callers ahead of you.
- Please have your service manual and a description of the problem available when you call.

1.3.1.2 Via FAX

- We give priority to phone inquiries, so we might need some extra time (up to two days) to provide you a satisfactory reply via FAX.
- If you send a FAX, please include the following information:

  Your complete name and address

  Your phone number

  Your FAX number

  The model and serial number of the product

  A complete description of the problem or request
- We may choose to call you by phone even when you send a FAX
- The FAX number for Critikon Technical Support is 1-813-286-7119

1.3.2 Repair Service

To obtain repair service, phone Critikon Repair Service Monday through Friday, 8:30 AM to 5:00 PM Eastern Time at 1-800-237-5591.

Please tell the person answering your call that you need Repair Service.

- State your:

  Hospital Name

  Address

  Telephone Number

  Model and Serial Number

  Complete Description of the Problem

- Critikon's Product Service Representative will advise you of the corrective action required. If you are advised to return the product to Critikon for repair, do the following:

  1. Package the product with adequate protection. If available, use the original materials shipped with the product.

  2. Include a brief description of the problem, as well as the name, address, and phone number of the person to be contacted for additional information.

  3. Include the Return Authorization Number (RA#) and a purchase order number.

  4. Ship the product, transportation prepaid, to the Product Service Center specified by your Product Service Representative. Repairs will be made at the service facility and the product will be returned to the purchaser prepaid.

1.3.3 Repair Parts

To obtain information on or to order repair parts, phone 1-800 237-5591 Monday through Friday, 8:30 AM to 5:00 PM Eastern Time.

Please tell the person answering the phone that you need Repair Parts.

1.4 PRODUCT DESCRIPTION

1.4.1 General Description

The 8700 series DINAMAP™ *PLUS* Vital Signs Monitors are portable devices used for noninvasive and invasive monitoring of patients in numerous clinical settings. Each Monitor can accompany patients to and from various hospital departments (emergency, radiology, recovery, cardiac step-down) and can be used during many specialized procedures in satellite areas, or during surgeries in physicians' offices or ambulatory surgery centers.

The Monitor can be battery powered when connected to an optional battery module, Critikon Reorder No. 8725. The Monitor can also run on AC power using a standard power cord.

The battery module uses two user-replaceable batteries. Battery usage is sequential; as the life of one battery diminishes, operation automatically switches to the other. The drained battery can be replaced with a fully charged spare for continuous and indefinite battery operation.

The Monitor is available in three models: Model 8700 features measurement of noninvasive blood pressure (NIBP) and blood oximetry (SpO2); Model 8710 adds ECG measurement to the features of the Model 8700; Model 8720 includes patient temperature measurements and has two invasive blood pressure measurement channels in addition to the features of the Model 8710.

1.4.2 Physical Description

The Monitor consists of the accessory kits and the monitor unit itself. The Monitor unit top assembly is comprised of the bezel, case, handle, mounting plate, and mounting hardware. When the top assembly is removed, the upper and lower frame assemblies are exposed.

The upper frame assembly includes the upper frame; keyboard assembly and cable; and display, mounting bracket, and cable. The pump assembly, pneumatic hoses and pump cable, speaker assembly and cable, muffler, and pump foam mount are also attached.

The lower frame assembly comprises the lower frame, connector assembly, fan assembly, power entry assembly and cables, and external dc connector and cable. The assembly also houses eight printed wiring boards, including the system processor board, pneumatics board, analog board, power supply board, battery switch board, DAS board (models 8710 and 8720), and motherboard.

1.4.3 Storage Batteries

The storage battery specified for use with the DINAMAP™ *PLUS* Monitor is a sealed lead-acid battery. It was selected for its high capacity (2.3 Amperes per hour for standard 10 hour rate), quick-charge ability (recharge time as little as two hours) and ease of replacement (has pressure contacts).

The expected battery cycle life is largely dependent on the way the battery is used. If the battery is allowed to be fully discharged after each use and then fully recharged soon after use, the battery should last for the full two hundred recharge life cycle. If a battery is used in the top one third of its charge and fully charged whenever possible, up to twelve hundred cycles can be expected, approximately six times the number of cycles used to 100% capacity.

A battery that has been fully discharged can be fully charged by the Monitor in less than five hours. If any storage batteries are in the battery module while the Monitor is connected to an external AC power source (even if the Monitor is off) the monitor will attempt to charge the batteries. If more than one battery is to be charged, the Monitor will automatically charge the second battery after the first battery either becomes fully charged or is removed from the battery module.

A fully charged battery can be stored up to six months and retain as much as 80% of its capacity. One fully charged battery will supply enough energy to operate the Monitor for approximately one hour. This operation would include continuous ECG, invasive blood pressure, temperature, pulse oximetery and non-invasive blood pressure operations set at five minute determinations.

Run Time	Typical Charge Time
10 min	45 min (0.75 hours)
20 min	90 min (1.5 hours)
30 min	135 min (2.25 hours)
40 min	180 min (3.0 hours)
50 min	225 min (3.75 hours)
60 min	270 min (4.5 hours)

1.4.4 Product Reorder Information

Model 8700 - NIBP and pulse oximetry

Includes monitor, power cable, adult DURA-CUF™ blood pressure cuff, 12-foot air hose, NIBP calibration kit, SpO2 sensor, SpO2 system cable, and operation manual.

Model 8710 - NIBP, pulse oximetry, and ECG

Includes monitor, power cable, adult DURA-CUF™ blood pressure cuff, 12-foot air hose, NIBP calibration kit, SpO2 sensor, SpO2 system cable, ECG cable, 3 ECG electrodes, 3 ECG lead wires, and operation manual.

Model 8720 - NIBP, pulse oximetry, ECG, temperature, and 2-channel invasive pressure

Includes monitor, power cable, adult DURA-CUF™ blood pressure cuff, 12-foot air hose, NIBP calibration kit, SpO2 sensor, SpO2 system cable, ECG cable, 3 ECG electrodes, 3 ECG lead wires, YSI temperature cable, and operation manual.

1.4.5 Accessory Reorder Information

1.4.5.1 Critikon Accessories

Accessories available from Critikon are listed in Table 1-1.

1.4.5.2 After-Market Accessories

The Monitor may also be used with certain equipment supplied by other manufacturers. For further information about the compatibility of such equipment, contact the Johnson & Johnson sales representative. The items listed below are known to have compatibility problems with the Monitor, and should not be used.

Transducers - The Monitor is not designed to work with 40μV/V/mmHg transducers such as Hewlett-Packard Models 267, 268, 1280, and 1290A.

Transducer cables - Viggo Spectramed cables with built-in preamplifiers that boost the signal of a 5μV/V/mmHg transducer to 40μV/V/mmHg and terminate in the H-P 12-pin connector will not work with the Monitor, even when connected by the Fogg Systems cable.

Intracranial pressure - The Monitor is not compatible with the Camino Intracranial Pressure transducers

The Monitor is also not designed to work with the following cables:

TC-HPO-2
TC-HPO-8040
TC-HPO-8030H
TC-HPO-8040H

1.4.6 Specifications

Monitor mechanical specifications are listed in Table 1-2, environmental specifications are listed in Table 1-3, and electrical specifications are listed in Table 1-4. Performance specifications are listed in Tables 1-5 through 1-10.

Table 1-1. Critikon Accessories

Accessory	Description
8725	Battery module, including 2 rechargeable lead/acid storage batteries
8726	Waveform printer module, including 2 rechargeable lead/acid storage batteries
8727	External battery charger, holds up to 4 batteries for fast recharge
8728	Heavy duty, woven nylon carrying case, with zippered main monitor compartment, three pockets with hook and loop closures for accessory items, carrying handle, and padded shoulder strap.
8729	Text printer module, including 2 rechargeable lead/acid storage batteries
8730	Thermal printer paper, 10 rolls per box.
8731	SpO2 system cable, for use with 9084 SpO2 sensor
8732	Domestic ECG cable kit, includes 3 (AHA red, black, and white) disposable electrodes, 3 lead wires, cable, instruction sheet
8733	Pole mount
8742	International ECG cable kit, includes 3 (AHA yellow, green, and black) disposable electrodes, 3 lead wires, cable, instruction sheet
9084	SensorMedics OMNI-SAT™ SpO2 sensor, for use with 8731 system cable

Table 1-2. Mechanical Specifications

ITEM	DESCRIPTION
MONITOR WEIGHT	9.8 lbs (4.45 kg) 6.2 kg
BATTERY MODULE WEIGHT	3.85 lbs (1.75 kg)
DIMENSIONS	9.25 inches high; 7.2 inches wide; 8.5 inches deep 23.5 × 18.3 × 21.6 cm
BATTERY MODULE DIMENSIONS	1.5 inches high; 7.2 inches wide; 8.0 inches deep 3.8 × 18.3 × 20.4 cm
ELECTROLUMINESCENT DISPLAY	320 by 256 pixels Viewing area 3.8 inches wide by 3.0 inches high
MOUNTINGS	Surface mount or optional pole mount

Table 1-3. Environmental Specifications

ITEM	DESCRIPTION
OPERATING TEMPERATURE	50° F to 104° F (10° C to 40° C)
OPERATING ALTITUDE	-1000 to 15,000 ft (-305 to 4570 m)
STORAGE TEMPERATURE	29° F to 167° F (-34° C to 75° C)
RELATIVE HUMIDITY	0 to 90 percent, noncondensing
LEAKAGE CURRENT	Less than 100 µA

Table 1-4. Electrical Specifications

ITEM	DESCRIPTION
AC INPUT VOLTAGE	88 to 268 VAC, 47 to 63 Hz
AC INPUT POWER	20-35 watts typical, including battery charger 70 watts maximum
AC LINE FUSES	2.0 A
DC INPUT VOLTAGE	8 to 32 VDC
DC INPUT POWER	15-21 watts typical; 42 watts maximum
BATTERY PACK OPERATION	Two batteries; sequential operation, one hour per battery, except 15 minutes per battery in NIBP mode Standard 10 hour rating is 2.3 Amperes per hour
POWER CABLE	Detachable, blue jacketed, 16 gauge, 10 foot length In USA, terminated in medical grade 3-prong plug International cable unterminated

Table 1-5. NIBP Performance Specifications

ITEM	ADULT DESCRIPTION	NEONATE DESCRIPTION
CUFF PRESSURE RANGE	0 to 250 mmHg	0 to 220 mmHg
INITIAL CUFF INFLATION	178 ± 15 mmHg	125 ± 15 mmHg
MAP DETERMINATION	20 to 225 mmHg	20 to 170 mmHg
SYSTOLIC DETERMINATION	30 to 245 mmHg	30 to 190 mmHg

Table 1-5. NIBP Performance Specifications (Continued)

ITEM	ADULT DESCRIPTION	NEONATE DESCRIPTION
DIASTOLIC DETERMINATION	10 to 210 mmHg	10 to 160 mmHg
DETERMINATION TIME	Manual/Auto Mode 20 to 45 sec typical; 120 sec maximum STAT Mode 19 sec typical at nominal blood pressure and heart rate	Same
OVERPRESSURE CUTOFF	300 mmHg +30, -48 mmHg	Neonate 235 ± 10 mmHg
PULSE RATE RANGE	40 to 200 mmHg	Neonate 40 to 220 mmHg
PULSE RATE ACCURACY	Within one standard deviation (68 % of all readings), or ± 3.5 %	Same
PRESSURE DISPLAY ACCURACY	± 3 mm Hg	Same
HEART RATE RANGE	40 to 200 bpm	Same
SYSTOLIC ALARM LIMITS	High 75 to 245 mmHg Low 30 to 150 mmHg	Same
DIASTOLIC ALARM LIMITS	High 50 to 210 mmHg Low 10 to 120 mmHg	Same

Table 1-6. ECG Performance Specifications

ITEM	DESCRIPTION
OVERLOAD PROTECTION	AC Voltage 1V p-p @ 60 Hz for 10 sec on all leads Defibrillator Protection Maximum 8 sec recovery from 5 kV Patient Connection Risk Current Less than 10µA Single Fault Risk Current Less than 50 µA
QRS DETECTION	Tall T Wave Rejection 100 % Range of Amplitude 0.5 to 5.0 µV; no response when less than 0.15 µV Range of Duration 70 to 120 msec; no response when less than 10 msec 60 Hz Voltage Tolerance (QRS=0.5 mV, 100 msec) 250 µV p-p Drift Tolerance Detect a QRS of 0.5 mV; 100 msec; 80 bpm w/o,1Hz; 4 mV triangle wave
HEART RATE METER	Range 10 to 250 bpm Accuracy ± 3 bpm, or ± 3 % of reading High Heart Rate Response Time Less than 5 seconds Low Heart Rate Response Time Less than 10 seconds
ALARMS	High Range Limit 80 to 250 bpm Low Range Limit 10 to 140 bpm Resolution of Settings 5 bpm
TIME TO ALARM	Tachycardia Less than 5 seconds Cardiac Standstill, 0 to 60 bpm Less than 5 seconds Low Heart Rate, 40 to 80 bpm Less than 10 seconds High Heart Rate, 80 to 120 bpm Less than 10 seconds
SPECIAL REQUIREMENTS	Input Dynamic Range ± 5 mV Input Impedance Greater than 2.5 Megohm System Noise Less than 20 µV p-p Multichannel Crosstalk Less than 1 % of input

Table 1-6. ECG Performance Specifications (Continued)

ITEM	DESCRIPTION
GAIN CONTROL	Gain Selection 40, 30, 30, 10, 5 mm per m Gain Switching Manual or Auto
TIMEBASE	Selection 50, 25, 12.5 mm per second Accuracy Within ± 10 %
OUTPUT DISPLAY	Minimum Channel Width 30 mm Aspect Ratio 0.4 ± 0.08 seconds per mV
ACCURACY OF SIGNAL	Maximum System Error ± 20 %, or ± 100 µV Frequency Response 0.5 to 40 Hz Maximum Hysteresis 0.5 mm Standardizing Voltage 1 µV Common Mode Rejection Less than 5 %

Table 1-7. SpO2 Performance Specifications

ITEM	DESCRIPTION
ACCURACY	± 1% at standard deviation; ± 2% at 90 to 99%; ± 3% at 75 to 89%; unspecified at less than 75%
SATURATION RANGE	40 to 99 %
PULSE RATE	30 to 250 bpm
PULSE AVERAGING	User selectable from 0 to 30 seconds in increments of 3 seconds; at power up, preset at 6 seconds
SATURATION PITCH INDICATOR	Pitch changes with saturation; tone volume selectable from maximum to completely silent.
SATURATION ALARM LIMITS	High 90 to 99%; low 40 to 95%

Table 1-8. IBP Performance Specifications

ITEM	DESCRIPTION
NUMBER OF CHANNELS	Two
RANGE	-30 to 300 mmHg
DISPLAY SCALES	Selectable in 10mmHg increments
TRANSDUCER SENSITIVITY	5μV/V/mmHg
GAIN ACCURACY	± 1% or ± 2 mmHg of reading, whichever is greater
GAIN DRIFT	± 0.42 mmHg per °C
ZERO ADJUSTMENT	±150 mmHg
ZERO ACCURACY	± 1 mmHg
ZERO DRIFT	± 0.23 mmHg per °C
BANDWIDTH	DC to 40 Hz
PULSE RATE RANGE	10 to 250 bpm
SYSTOLIC ALARM LIMITS	High 20 to 300 mmHg Low 30 to 150 mmHg
DIASTOLIC ALARM LIMITS	High 20 to 300 mmHg Low 30 to 120 mmHg
MEAN ARTERIAL PRESSURE ALARM LIMITS	High 20 to 300 mmHg Low 30 to 120 mmHg

Table 1-9. Temperature Performance Specifications

ITEM	DESCRIPTION
CONNECTOR	YSI 400 compatible
RANGE	89.6° F to 107.6° F (32° C to 42° C)
SCALE SELECTION	°F or °C
ACCURACY	± 0.1° C, not including tolerance of probe
RESOLUTION	0.1° C or 0.1° F
SELF TEST	37.1 ± 0.1 °C (98.8 ± 0.4 °F) internal, manual
ALARM LIMITS	High 89.6° F to 107.6° F (32.0° C to 42.0° C) Low 89.6° F to 107.6° F (32.0° C to 42.0° C)

Table 1-10. Alarm Functions

ITEM	DESCRIPTION
SYSTEM ALARM INTERNAL TEST	Performed at power up and during operation
NIBP PROCEDURAL ALARMS	Overpressure Excess determination time Excess pump-up time Lack of determination
OXYGEN SATURATION PROCEDURAL ALARMS	Low signal Probe disconnection Probe failure
VOLUME LEVEL	Selectable from minimum to maximum on all parameters

SECTION 2. THEORY OF OPERATION

2.1 INTRODUCTION

This section contains theory of operation for the Monitor. Overall operation is described in paragraph 2.2. Refer to paragraph 2.3 for a description of each functional system. Detailed theory for each circuit board is provided in paragraph 2.4.

2.2 SYSTEM THEORY OF OPERATION

A system block diagram of the model 8720 Monitor is shown in Figure 2-1. The patient vital signs are measured by a variety of electronic sensors. The non-invasive blood pressure and pulse oximetry measurements are controlled by the analog board. The Data Acquisition System (DAS) board provides a similar function for the invasive blood pressure, ECG, and temperature measurements. The sensor measurement operations of each board are supervised by the system processor, which converts the results into visual and aural presentations at the electro-luminescent display and audio loudspeaker.

Operator access is via a keyboard, and an interface accessory is available to provide a hard copy printout from an optional printer. Data interchange between the system processor program and a host computer is provided by a communications interface.

The Monitor includes a pneumatics system required for NIBP operation. The pneumatics board regulates the operation of the pneumatic pump, valves, and cooling fan. The Monitor can be operated from ac power, storage batteries, or an external dc power source. The power supply board rectifies the ac power, recharges the batteries, and provides regulated dc operating power for the Monitor. The battery switch board provides power supply monitoring and control under supervision of the system processor.

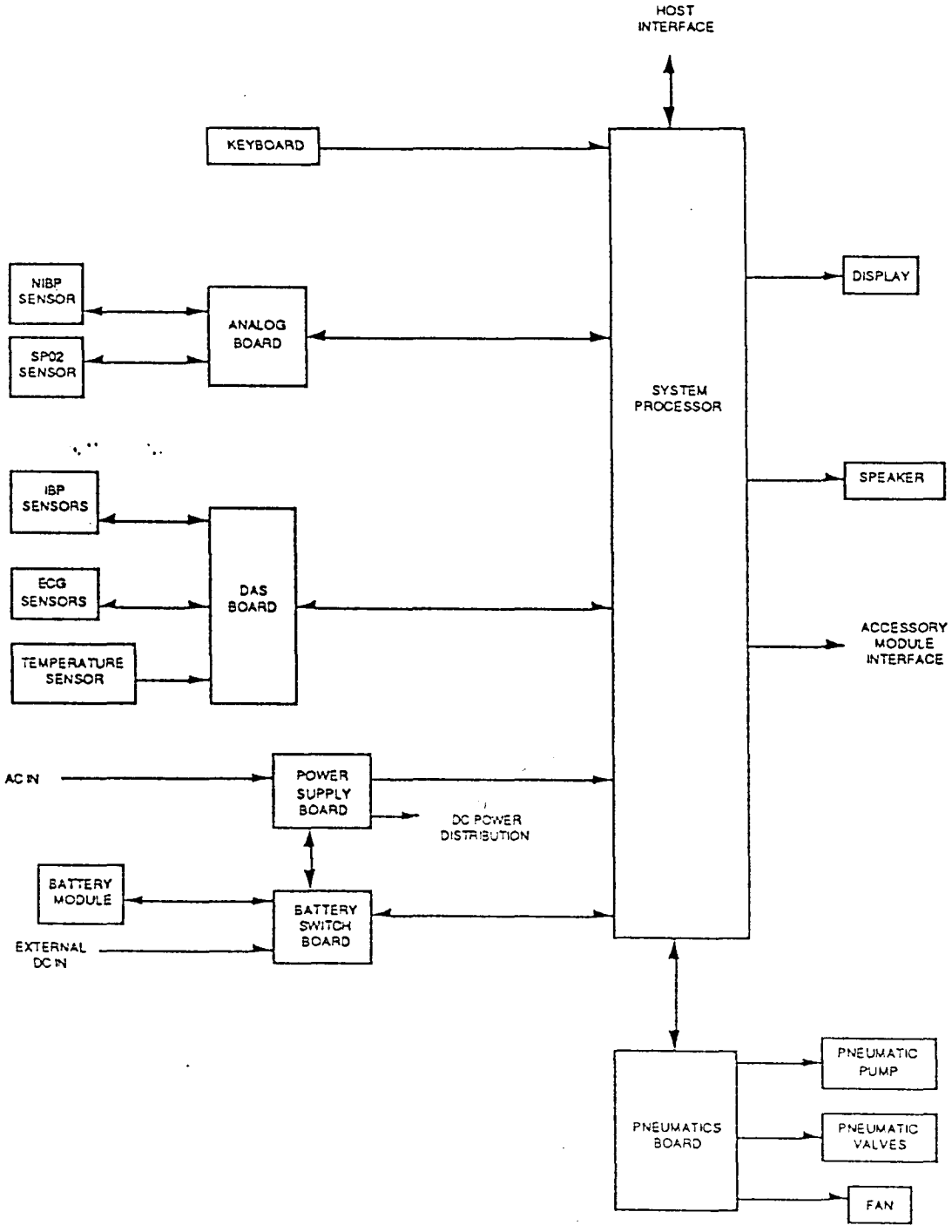


Figure 2-1. Model 8720 System Block Diagram

Models 8700 and 8710 Monitors differ from the above description in that the invasive blood pressure and temperature channels are not available, and the ECG channel is also not available on the Model 8700.

2.3 FUNCTIONAL THEORY OF OPERATION

The following paragraphs provide a simplified description of each of the Monitor functional systems. Foldout (FO) diagrams are located at the end of this section. Information about input and output sources and destinations, along with connector pin identifications, is included as an aid to troubleshooting. Refer to paragraph 2.4 for complete circuit details.

2.3.1 System Processor

The system processor (Diagram FO-1) is based on Motorola 68302 microprocessor (CPU) U41. The microprocessor incorporates failsafe logic that causes the Monitor to enter a safe state if microprocessor operation ceases.

RAM consists of 256K bytes of battery backed read-write memory. To maintain RAM contents, the memory logic supply, controlled by supervisor U40, automatically switches to the battery supply in the event of power failure. The program storage ROM consists of single socket U36 for 16-bit word EPROM or PROM devices. EEPROM U1 contains the NIBP pressure calibration constants and unit model number used to configure the Monitor for the appropriate parameter set and language option. A real time battery-backed clock is provided that allows the user to set time and date for time stamping for trend displays and for waveform and tabular printouts.

The system processor communicates with the DAS board via 62.5K bit/sec serial bidirectional CMOS interface U30. Additional interfaces provide digital inputs and outputs with the analog board, pneumatics board, battery switch board, and power supply.

The CPU is provided with a serial communications interface to an external host. Receive data, transmit data, and clock signals are routed via host buffer U28. Baud rates are software programmable from 300 to 76.8K bits/sec. The system processor also has a bidirectional serial interface to an optional graphics array printer or other serial device. The bit rate is programmable from 300 to 76.8 bits/sec.

The electroluminescent display is managed by Hitachi HD63484 advanced CRT controller (ACRTC) U31. The display image is a composite of overlaid foreground and background screens. The graphics subsystem has 128K x 16 bit RAM U34, U35 to store graphics images. Graphics images for alphanumeric and special characters are handled directly by the software.

The microprocessor includes audio tone generator U43, used for alarms, QRS detect tones, audio key feedback, and proportional pulse tones related to SpO2 saturation level. Frequencies and volume levels of the audio tones are software selectable at U42.

2.3.2 Data Acquisition System

The data acquisition system (FO-2) for Model 8720 incorporates subsystems for invasive blood pressure, ECG, and temperature signal processing. Model 8710 uses only the ECG subsystem. Overall operation of the DAS is controlled by DAS CPU U1. Patient vital sign measurements and DAS status and error conditions are relayed to the Monitor system processor via J7-2 from isolated serial port U5. The system processor sends initialization, calibration, configuration, and test commands to isolated port U6 via J7-1. The channel inputs to multiplexer U9 are routed to U7 for conversion to the digital format required for CPU processing.

The patient temperature is sensed by the value of the transducer resistance applied to test switch U27 via relay K1. The relay allows the system to compare this input with that of a precision resistor for self testing. The test switch is used to help determine what gain errors exist in amplifier U8. The amplified signal is applied to one of the inputs of multiplexer U9.

The patient blood pressure is sensed by the resistive bridge transducer connected to either of the two invasive pressure channel inputs. Transducer excitation is buffered from the +5 volt supply. Each transducer input is applied to a test switch that allows a self test signal to ensure channel gain and offset accuracy. The instrumentation amplifier (IA) output is then filtered and passed to multiplexer U9.

Patient ECG is measured by a three lead sensor connected to an input protection network. The network protects the input from interference from electrosurgical noise and defibrillator voltages. A lead switch circuit allows the DAS CPU to switch the input among the three standard ECG sensor leads, as selected by the user from the front panel. The lead fail circuit and common nulling loop provide lead compensation that ensures the accuracy of the ECG measurements. The instrumentation amplifier output is filtered by a network that employs a fast charge control circuit that maintains the filter time constant.

The DAS power supply provides for patient isolation from earth ground. The supply consists of medical grade dc to dc converter PM1 and four linear voltage regulators. A shutdown command from the Monitor system processor is applied to PM1 from J7-1 via Q6 to save power when the DAS functions are not being used.

The output from +5 volt supply regulator U18 is monitored by U16, and any undervoltage swings result in a DAS reset command from U16. A POWER OK signal from the regulator is also monitored by the DAS CPU for voltage errors or if current or thermal limits are exceeded at U18. The POWER OK signal from +9 volt supply regulator U15 operates similarly. The -9 volt output from regulator U17 is monitored for errors by the multiplexer. Any faults that may occur in the -5 volt supply provided by regulator U25 are detected by errors at the ADC.

2.3.3 Pulse Oximetry System

The pulse oximetry system (FO-3) provides continuous readings of oxygen saturation and pulse rate. The physiological signals produced by a photodiode in the oximeter sensor are applied to the analog board at J2-7 and amplified by U9 and U10. The signals are then fed to synchronous demodulator U17. After filtering by amplifier U19, the demodulated saturation signals MIR and MRED are routed to the Monitor system processor for A/D conversion. The sensor pulse component of the sensor signals is amplified by U19 and routed as LIR and LRED to the system processor. An adjustable offset voltage to U19 is set by DAC U20. The DAC output is controlled by digital data inputs PD0 through PD7 enabled by DAC STB 0 at J1-36. The master clock for the pulse oximetry subsystem is routed from the system processor to the analog board via J1-20.

The analog board also provides software-controlled adjustment of the AC drive current to the LEDs in the oximeter sensor. Power is supplied to the sensor interface by a push-pull switching power supply. U15 controls the current limit and on/off functions of the isolated power supply. The +10 volt power supply Q6, Q13 is derived from the master clock signal. Presettable binary counter U16 provides the carrier frequency reference clock for synchronous detector U17. The current flow from Q6, Q13 is monitored by the system processor via the PA monitor output from J1-18. The -12 volt power supply Q12, Q15 is also derived from the master clock. The system processor is provided -12 volt operating power via J1-5, 7.

Each sensor type (adult/pediatric or neonatal) contains a unique resistor connected at J2-4. The resistor value is read by A/D converter U36 and converted to bit serial data that is applied to opto-isolator U3. The data is then applied via J1-38 to the system processor to enable the appropriate selection of monitoring mode.

2.3.4 NIBP System

The noninvasive blood pressure system (FO-4) uses the oscillometric technique to measure blood pressure and pulse rate. The signals from the pressure sensor are applied to preamplifier U23 within the analog board. Any of four types of pressure sensors can be used, as configured by jumpers and resistors. An unfiltered transducer output signal PT is routed to the system processor via J1-17. The signal is amplified and filtered to extract the pulse component. Low pass filtering is provided by U24-14, and the signal is then applied to high pass filter U24-8 and clamp U26. The filtered signal is routed to the system processor via J1-16. Addressable latch U22 is used to switch circuit gain between the adult/pediatric and neonatal monitoring modes.

The magnitude of the transducer amplifier offset from scaler/buffer U24-7 is software-adjustable by DAC U20 for auto-zero. Transducer excitation current or voltage for the pressure sensor is software adjustable for scale calibration. The magnitude of the excitation produced by current driver Q1, Q2 is set by DAC U20. The DAC scale and offset outputs are controlled by digital data inputs PD0 through PD7 enabled by DAC STB 0 at J1-36.

The system software includes an internal online self-test feature for the FPT channel at power-up and after each non-stat mode determination. Additionally, buffer U25-7 provides a measurement of the transducer excitation to the system processor for calibration verification.

2.3.5 Pneumatics System

The pneumatics system (Figure 2-2) provides air pressure for the NIBP cuff, manifolding for control of the cuff pressure, and an overpressure signal sent to the system processor in the event pressure exceeds about 300 mm Hg. The system comprises an air pump, check valve, overpressure switch, power control circuit, and three solenoid-operated pneumatic valves. The pneumatics board provides control of the pneumatic pump in accordance with commands received from the system processor.

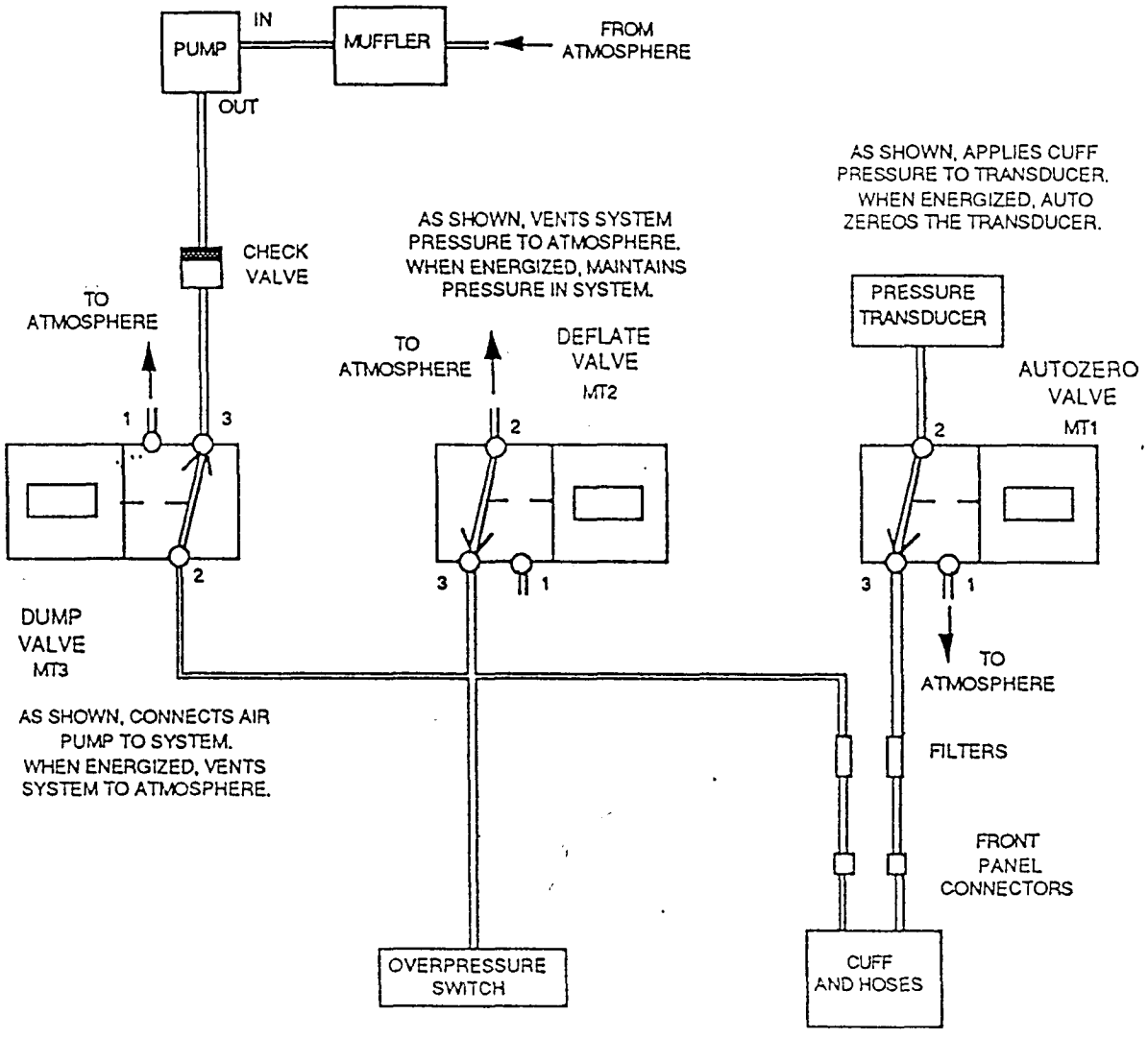


Figure 2-2. Pneumatics System Simplified Schematic

The rotary-driven diaphragm pneumatic pump is operated by pulse width-modulated dc voltages supplied by the interface circuit. The pump is mounted within a reinforced-plastic air pressure storage vessel. Air from the pump output is routed to the inflate valve port. It is then ported to the cuff output manifold.

FO-5 is a simplified diagram of the pneumatics system control circuits. The pump on command from the system processor is processed by logic U2, U3. The logic turns on Q2 to activate the pump. The pump enable signal is also applied to the fan circuit to prevent excessive power supply loading by disabling the fan until pump operation ceases.

The normally deenergized Zero valve MT1 allows cuff pressure to be applied to the NIBP sensor. When a command from the system processor is processed by logic circuit U2 and U3, Q3 turns on, energizing MT1 to maintain cuff network pressure while opening the transducer to ambient pressure.

Deflate valve MT2 is normally energized when an enable command from logic U2, U3 turns on Q8 to maintain system pressure in the cuff. When a deflate command from the system processor is processed by logic network U2, U3, the deflate valve deenergizes and ports the cuff network to atmosphere.

The normally deenergized dump valve MT3 connects the air pump to the cuff network. When a dump command from the system processor is processed by logic circuit U2 and U3, Q4 turns on, energizing MT3 to port the network to atmosphere.

If system overpressurization occurs, a signal from closed switch S1 (or S2) is applied to logic U2, U3 via U4-1. The logic then energizes the dump valve and deenergizes the deflate valve. An overpressure signal sent to system processor via J1-13 generates visual and audible overpressure alarms. U2, U3 also turns on Q7 during the overpressure condition to ensure the dump valve is energized if Q4 fails. If excessive current is drawn at any time by the pump, a sense signal from Q2 is applied to U4-2. The resulting input to U4-1 results in the same actions described for an overpressure condition.

After a pump shutdown due to overpressure or overcurrent, logic U2, U3 can be reset by the pneumatic reset signal from the system processor. When a fail safe alarm signal is sent to logic U2, U3 from the system processor, the dump valve is energized, the deflate valve is deenergized, and the pump drive circuit is disabled.

Internal temperature is limited by a fan under the control of Q6, comparator U14-14, and thermistor RT1. If an overtemperature conditions occurs, the second comparator output at U14-13 signals the event via J1-5. Valve sense signals from Q3, Q4, and Q8 are applied to the system processor only for use by the factory during manufacturing tests.

2.3.6 Power Supply

The Monitor power supply system, comprised of components of the power supply board (enclosed in dashed lines) and battery switch board, is illustrated in FO-6. Ac power applied to the line power converter within the power supply board provides a nominal +18 volts dc bus. The presence of the +18 VDC bus is sensed by the system processor via U3-2. The +18 Vdc bus also supplies the voltage that lights the front panel mains indicator.

The power supply DC SOURCE bus can be supplied by external dc power, from either storage battery, or from the power supply board +18 volt bus. An external dc power source is coupled to DC SOURCE by CR4. Overcurrent protection is provided by F1, and CR22, Q27 and R2 are used for overvoltage and reverse-polarity protection. The external dc power input is monitored by the system processor from the voltage drop across R52 and R23. The output from storage battery 1 is switched to DC SOURCE by MOSFET Q24 under command of the USE BATT 1 input from the system processor. The output from storage battery 2 is switched to DC SOURCE by MOSFET Q25 under command of the USE BATT 2 input from the system processor.

The power supply internal VB bus is powered by either storage battery via CR13 and CR14 or from the power supply board +18 volt bus via CR16. Internal +5 volt regulator U4 is powered by the VB bus via CR18 or from the external dc source via CR17.

Battery charger current, derived by Q20, U6 from the +18 Vdc bus, can recharge two storage batteries within 12 hours. Battery charge monitoring and control are provided by a circuit that includes U5-1 and U5-7 on the power supply board and U5, U6, U7, U8, U9 on the battery switch board. MOSFET Q17 applies charging current to storage battery 1, and MOSFET Q19 applies charging current to storage battery 2. The battery charge can be maintained indefinitely without damage to the batteries as long as the Monitor is connected (either switched on or off) to the ac power source.

Storage battery 1 is switched to the test load resistor R1, the equivalent to powering the pneumatic pump motor, by MOSFET Q18 under command of the TST BATT 1 input from the system processor. Storage battery 2 is switched to R1 by MOSFET switch Q20 under command of the TST BATT 2 input from the system processor. Battery test load current is monitored by the system processor from the voltage drop across R39 and R19.

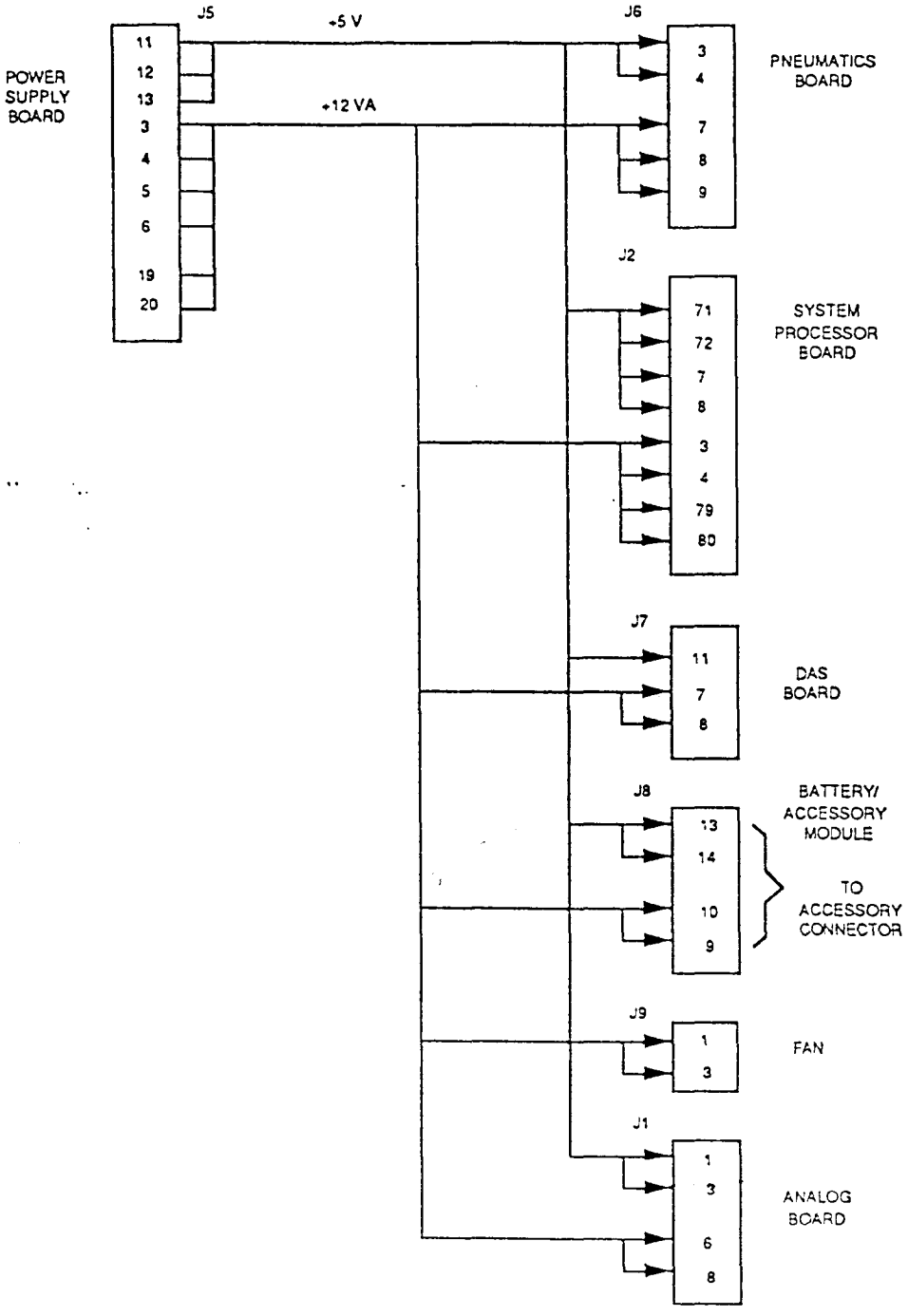


Figure 2-3. Power Distribution Diagram

The low voltage power supply provides regulated +12 V and +5 V outputs to the power distribution system from the DC SOURCE bus. Power distribution within the Monitor is shown in Figure 2-3. An additional power source of -12 Vdc to the system processor from the analog board is described in paragraph 2.3.3.

Power supply on/off control is provided by logic circuit U2, which receives set/clear commands from the front panel mains switch. The logic circuit controls battery switch board operation by commands to the internal +5 Vdc voltage regulator, and applies a shutdown signal to the distribution power supply within the power supply board via U2-14. The shutdown signal is also sensed by the system processor via CR24. A signal from Q16 also switches logic U2 to off to prevent a weak battery from cycling power on until the mains switch is again pressed on.

2.4 SCHEMATIC DESCRIPTIONS

A detailed circuit description of each of the main circuit board assemblies is provided by the following paragraphs.

2.4.1 System Processor Board

The system processor board circuits are shown on schematic SC315-332 contained in Section 4. The system processor is based on Motorola MC68302 Integrated Multiprotocol Processor U41. The 68302 includes a 68000 microprocessor core, a systems integration block, and a communications processor. The 68000 processor core is a low power HCMOS implementation of the MC68000. The system integration block consists of a DMA channel, an interrupt controller, two parallel I/O ports, 1152 bytes of dual port static RAM, three programmable timers, four chip select signals with wait state generation logic, and a clock generator. The communications processor consists of a RISC controller, three serial communications controllers which support UART, HDCL/SDCL, BISYNC, and DDCMP protocols, a synchronous communication channel, and six DMA channels.

The system clock is generated by 16.000 Mhz crystal Y1 and the 68302 internal clock generation circuitry. The clock signal is available at CLKOUT (U41-98) and at test point TP3. Reset signal generation is provided by MAX695 supervisor circuit U40. Its low true output RESET-0 (U40-15) is inverted with one section of 74HC04 U14, then inverted again with two sections of 74HC03 open drain NAND gate U13. The outputs of these NAND gates are connected to RESET-0 (U41-92) and HALT-0 (U41-91) of the 68302. The MAX695 asserts RESET-0 for a minimum of 140 milliseconds after +5V reaches 4.75 V on power up. SYS_RESET-0 is connected to J2 at pin 60.

The IDMA channel is configured for externally-requested transfers to and from the 63484 graphics controller U31. The control signals DMA request [DREQ-0] (U41-69), DMA acknowledge [DACK-0] (U41-70), and DMA done [DONE-0] (U41-71) are connected to similar pins on the graphic controller.

Four programmable chip signals are available on the 68302. Each has selectable base address, block size, read only, write only, or read-write options, and DTACK/wait state generation. CS0-0 (U41-128) is used to select the program memory EPROM U36 (ROMCS-0). It must be configured for read only operation, and internal DTACK generation. One wait state is required with 150 nsec EPROMs. CS1-0 (U41-127) selects the static RAM (RAMCS-0). It must be configured for read-write operation, and internal DTACK generation. No wait states are required for 85 nsec RAM devices. CS2-0 selects the graphics controller (ACRTCCS-0). It must be configured for read-write operation and external DTACK generation. CS3-0 (U41-126) is used to select IO device address space. It receives additional decoding with 74HC138 U19 and address signals A12, A13, and A14 to provide eight chip selects in 4K byte blocks. CS3-0 must be configured for read-write operation with internal DTACK generation and two wait states.

The interrupt controller is configured to accept requests from internal (on-chip) and external sources. Internal sources are the communication processor and its DMA channels, the IDMA channel, and the internal timers. The external sources are VSYNC-0 and ACRTCIRQ-0 from the graphics subsystem, BPRT_SYNC-0 from the printer interface, and the power fail signal BPFI-0. Full priority control and vector generation are available in the interrupt controller.

The three serial channels of the 68302 communications processor are all used in UART (asynchronous) mode. Channel one is connected through inverting HC buffers to the host communications connector J4. Bidirectional serial data (RXD1, TXD1) and control signals (CD1,CTS1-0, RTS1-0) are available. Channel two transmit and receive data signals are connected through 74HC541 buffer U30 to the printer via mother board connector J2. Serial transmit and receive communications with the DAS subsystem using channel 3 are also buffered by U30.

2.4.1.1 Failsafe Logic

A latch for the failsafe signal is formed by cross-coupled NAND gates (U13). These devices are open drain, and both their ouputs are pulled up to +5V with 10k ohm resistors of network U45. The active low output of the latch (FAILSAFE-0) is available at J2-17. The latch is cleared by asserting SYS-RESET-0, and set by a low pulse from either the 68302 internal watchdog timer signal WDOG-0 (U41-117) or the gated clock calendar DS1284 TWD-0. WDOG-0 is an open drain output, and is pulled to +5V with a 10k ohm resistor in network U26. The watchdog timer output from DS1284 clock calendar INTB (U8-26) is gated with the Q-0 output of cross-coupled NAND latch U11 to generate TWD-0. This latch is cleared by SYS_RESET-0 and set by DAS_TXD, preventing the DS1284 from setting the failsafe latch until the first serial transmission is sent to the DAS subsystem. The WDOG-0 and TWD-0 signals are logically ORed using 74HC08 U16.

When FAILSAFE-0 is asserted, 74HC125 tri-state buffer U18 is enabled, allowing the 1kHz square wave from the DS1284 clock calendar (U8-23) to be driven through 10k ohm resistor R65 into the input of TLM082 audio amplifier U15, producing an audible warning.

FAILSAFE-0 is also an input to ZDEAMANB pin U9-4 of the ACRTC support gate arrray. When asserted, output clock Z115KHZ (U9-68) is disabled, and all serial video data is output on ZPIXDAT (U9-65) following the sixteenth ZPIXHSB (horizontal sync) pulse after the rising edge of ZPIXVSB (vertical sync) is logic zero. This blanks the display except for the top sixteen rows.

2.4.1.2 Read-Only Memory

Program storage consists of a single socket (U36) for word-wide (16 bit) EPROM or PROM devices. The device supports 1MEG (64Kx16), 2MEG (128Kx16), or 4MEG (256Kx16) devices. Chip select is provided by ROMCS-0 (U41-128). This output from the 68302 programmble chip select logic should be configured for base address = 0, read only operation, with the block size set to the corresponding device size. With 150 nsec access time EPROM/PROMs, one-wait state operation is possible. With 100 nsec or faster parts, the system can operate with zero-wait states. The OE-0 signal at U36 is generated by ORing of LDS-0 and UDS-0 using 74HC08 U10. Note that the chip select and output enable logic is not fully decoded with respect to read/write external to the 68302. Therefore, unless the 68302 is programmed for read-only operation, a write to the EPROM/PROM address space will cause data bus contention.

2.4.1.3 Read/Write Memory

256K bytes of battery-backed read write memory are provided. 128K-by-eight low power static RAM devices U32 and U33 are organized as 128K-by-sixteen bits. U32 contains the upper bits (D8-D15) and U33 contains the lower bits (D0-D7). The RAM is powered by +5V2, provided by the +5V logic rail or the lithium battery voltage, whichever is greater. +5V2 is selected by MAX695 processor supervisor U40-2.

Chip select for the RAM devices is generated by ANDing 68302 programmable chip select logic output RAMCS-0 (U41-127) with MAX695 output WPCE-0 (U40-12) using 74AC32 U2. WPCE-0 goes low only when +5V is greater than +4.65V, thus providing protection against writes to the RAM during power up and down transitions. 74AC32 AND gate U2 is powered by +5V2 to assure minimum battery consumption by driving CS1-0 (U32-22, U33-22) to within 0.1V of +5V2 during power off.

Output enable for U32 is generated by ANDing UDS-0 with the inverted R~W-0 (74HC04, U14) using one section of 74AC32 U5. Output enable for U33 is similar, ANDing LDS-0 with the inverted R~W-0 using one section of 74AC32 U3. Write enable for U32 is generated by ANDing UDS-0 with the R~W-0 using one section of 74AC32 U5. Write enable for U33 is similar, ANDing LDS-0 with R~W-0 using one section of 74AC32 U3.

2.4.1.4 Serial EEPROM

93C46 serial EEPROM U1 provides 1024 bits of non-volatile memory organized as 64 sixteen-bit words. Interface to the 68302 is via the Serial Communication Port (SCP) in the communication processor. The SCP is a three-wire synchronous interface, providing receive data, transmit data, and clock signals.

The EEPROM is selected by asserting output Q0 of 74HC259 bit addressable latch U20-4. Data and instructions are clocked into the EEPROM DI pin (U1-3) on the rising edge of EECLK (U1-2). Data and status information is clocked into the SCP on the falling edge of EECLK. The maximum bit rate for the EEPROM is 700kHz.

2.4.1.5 Analog Input Subsystem

A sixteen channel, 12 bit analog input subsystem is based on MAX172 successive-approximation analog-to-digital converter (ADC) U37. The ADC includes on chip voltage reference generation (-5.25V), a 0 to +5V input range, (1 LSB = 1.22 MV) and 13 microsecond maximum conversion time. The 1 MHz conversion clock is generated by the graphics support gate array (U9-31) by dividing down the system clock. The digital output of the MAX172 is isolated from the processor data bus by 74HC541 tri-state buffers U29 and U47. This isolation decreases the coupling of high speed bus digital noise into the conversion circuits. A conversion is started, and the previous result driven onto the data bus by reading address CS3 + 0x2000. The end of a conversion is signalled by the negating of low true BUSY-0 (U37-22), which is connected to Port A bit 7 of processor U41.

MAX358 eight-to-one analog multiplexers U38 and U39 are joined to create a 16-to-one multiplexer. Analog channel selection is controlled by latched address bus signals A3 thru A6 using 74HC377 latch U25. Latched A6 is connected directly to the OUTPUT ENABLE pin of U38, and through 74HC04 inverter U14 to the OUTPUT ENABLE pin of U39. This establishes U39 as the lower eight channels, and U38 as the higher eight. Channel selection within each device is controlled by latched A3, A4, and A5. Latch U25 is accessed by reading address CS3 +0x3000+ (valid select data).

Multiplexor settle time to 12-bit accuracy is 3.5 microseconds. The MAX358 is guaranteed to have break-before-make switch action within each device. However, feedthrough may occur when a new channel is selected from the other device.

The outputs of the two MAX358s are connected to the input of SHC298 sample-and-hold amplifier U44. The input signal is connected to 1000 pF capacitor C19 when CONT_INP (U41-8) is logic high (SAMPLE), and disconnected when CONT_INP is low (HOLD). Acquisition time to 12-bit accuracy is 10 microseconds maximum. CONT_INP is connected to latched address signal A2 via latch U25. The OUTPUT (U44-5) of the SHC298 is connected to the analog input (U32-1) of converter MAX172.

2.4.1.6 Graphics Subsystem

The graphics subsystem is designed to drive a 320-by-256 monochromatic, electroluminescent (EL) display panel. The subsystem consists of the HD63484 graphics controller, a logic support gate array, video memory, and support buffers and logic.

HD63484 advanced CRT controller (ACRTC) U31 offloads from the system processor the tasks of graphics and character generation and control of the display device. The 68302 communicates with either the ACRTC (using normal bus cycles) or with the IDMA channel. OR gates of 74AC32 U4 and flipflop 74AC74 U6 decode chip select logic for the normal and DMA interface.

ELVLSI logic support gate array U9 is a CMOS ASIC that decodes ACRTC to video memory accesses and serializes graphics bit data for transfer to the EL panel. In addition, it provides display blanking during system failures and division of the system clock.

The video memory consists of two 128k-by-8 bit static RAMs organized as a 128k-by-16 bits wide. Interface signals to the EL panel are located at connector J5. They are buffered version of VIDEO_DATA, VIDEO_CLK,VIDEO_HS (Horizontal Sync), and VIDEO_VS (Vertical Sync).

2.4.1.7 Realtime Clock

A battery backed DS1284 realtime clock device U8 provides time of day and calendar information. The device is powered from the logic power rail when available, or from 3.7V (nominal) lithium battery B1 when the system is powered down. The DS1284 includes internal oscillator circuitry which provides a stable timebase using 32768 Hz crystal Y2. The DS1284 byte wide registers are located at odd bytes starting at CS3+0x4000. Write protection of these registers during power transitions uses the WPCE-0 output from MAX695 processor supervisor U40, gated with LDS-0 and R~W-0 using always-powered 74AC32 U2. The watchdog alarm features are used in the failsafe logic circuits described above.

2.4.1.8 Audio Subsystem

An audio subsystem is included to generate sound for rate detection, key annunciation, and alarms. It consists of an programmable sinewave generator, an logrithmic attenuator amplifier circuit, an output amplifier, and an enable circuit. It is a single channel system designed to drive an 8-ohm speaker.

ML2036 programmable sinewave generator U43 produces a sinewave output of approximately 5 volts peak to peak centered on +5V_RET. The output frequency is the programmed (serial) 16 bit data word divided by four. The ML2036 uses a 4 MHz clock, which is the 16 MHz system clock divided by four in graphics support gate array U9. The ML2036 is interfaced to the 68302 via the write only Serial Communication Port (SCP) and two digital control signals. TCLKEN-0 controls the synchronous clock from the 68302 (U41-77). It is an output from 74HC259 addressable latch U22. When asserted, it turns on 74HC125 tri-state buffer U18, which enables the clock signal to the ML2036 SCK input (U43-6). The output of the 74HC125 buffer is pulled to the logic rail through 10k ohm resistor R4. Serial data is clocked into the ML2036 on rising edges of SCK. TLATCH controls the ML2036 data latch. It must be high during serial data transmission, and latches the data on its falling edge. TLATCH is an output of 74HC259 addressable latch U22. Because the 68302 SCP is an 8-bit device, two writes are required to set the frequency. The ML2036 expects the data to be shifted least significant bit first.

ML2009 logarithmic attenuator/gain amplifier U42 provides volume control for the audio system. It provides up to 44 dB of dynamic range with sixteen levels each of attenuation and gain. The output level is selected by a 5-bit word using 74HC377 latch U24. The input to the latch is the system address bus, where A7 selects attenuate (logic hi) or gain (logic low), A3 through A6 select the sixteen levels, and A1 acts as the write strobe (WR-0). Multiple writes to the latch (located at CS3+ 0x6000) are required for proper programming, first with A1 low, then with A1 high.

The output amplifier consists of two stages of TL082 op amp U15 and discrete transistor pair Q2 and Q4. The ML2009 output feeds the first stage of U15 in a inverting gain-of-2 configuration. The second U15 stage is a unity gain stage with a 5 volt offset added. The output of the second stage drives the bases of transistors Q2 and Q4, which are in a push-pull arrangement. 10 k ohm resistor R60 provides feedthrough near the switch point to reduce distortion.

The bases of Q2 and Q4 are also driven by the output of 74HC125 tri-state buffer U18 to emit an audible alarm if a failsafe occurs. The emitters of the Q2/Q4 pair are coupled to speaker connector J1 through 100 microfarad capacitor C5. An audio enable circuit controlled by digital output Q7 of 74HC259 addressable latch U20 switches the AUD_RET (J1-2) to +5V_RET when N-channel MOSFET MTD5N05 is turned on.

2.4.1.9 Keypad Interface

An interface to a matrix-encoded keypad is provided at connector J3. The circuit consists of three output strobe signals and four input sense signals. The strobe signals (KBCOL0,KBCOL1, and KBCOL2) are active low outputs from 74HC259 addressable latch U20. These outputs are series diode protected to eliminate shorts during multiple key closures. The sense signals (KPROW0, KPROW1, KPROW2, and KPROW3) are pulled to the logic rail through 2.8k ohm resistors and buffered with three sections of 74AC810 U7 and one section of 74HC08 U16. The non-inverting output of these buffers (BKPROW0, BKPROW1, BKPROW2, and BKPROW3) connect to digital I/O port B bits 0 through 3 of the 68302 microprocessor.

2.4.1.10 Digital Inputs

All digital inputs are read by bits in ports A or B on the 68302. These inputs are isolated by buffers or logic gates.

2.4.1.11 Digital Output Ports

Two octal output ports are provided that interface to a four channel DAC and two addressable latches on the analog board, but also can be used for general purpose output. The lower 8-bit system data bus is latched by 74HC377 U26 during writes to CS3 +0x7700. The outputs of the latch are available as PD0 - PD7 at pins 50 through 57 of connector J2.

Eight bits of the address bus are latched by 74HC377 U27 during writes to CS3+ 0x7000 +value. The low order address values (A1, A3 through A6, A8 through A10) are dependent on the desired output value. DAC_STB-0 (latched A1) is at J2-43. LATCH_DATA (latched A3) is at J2-47. CHSEL0 (latched A4) is at J2-44. CHSEL1 (latched A5) is at J2-45. CHSEL2 (latched A6) is at J2-46. POLATCHSEL-0 (latched A8) is at J2-48. BPLATCHSEL-0 (latched A9) is at J2-49. X_OUT (latched A10) is at J2-38.

74HC259 bit addressable latch U21 provides eight digital outputs to connector J2. The device is selected by byte reads to even addresses at CS3+ value, with A3, A4, and A5 selecting the output bit and A1 providing the data. 74HC259 latch U20 is addressed like U21, except using odd addresses at CS3+ 0x1000 +value. It provides three outputs to connector J2, plus the three keypad strobes described above. U22 is an additional 74HC259 latch addressed in a similar manner, with its base at CS3+0x1000 +value using even addresses.

2.4.2 DAS Board

The DAS board circuits (Models 8720 and 8710 only) are shown on schematic SC315-370 contained in Section 4. The DAS board contains components of the Data Acquisition System (DAS), including the following subsystems:

The Microprocessor (DAS CPU), Opto-isolators, and control logic

The Analog to Digital Converter (ADC) and multiplexer

The ECG channel and lead switching

The two Invasive Blood Pressure (IBP) channels

The temperature channel

The isolated power supply

The physiological signals are acquired, amplified, and filtered, after which they are converted to digital values. Further signal processing occurs on the digital values to perform QRS detection, pacemaker spike rejection, and further conditioning of the IBP and temperature signals. The processed data is then sent to the Monitor system processor along with DAS status and error conditions. DAS receives commands from the Monitor system processor to configure the ECG leads, calibrate the pressure channels, check the temperature channel, and initialize the DAS system. For patient safety, the entire DAS system is electrically isolated from earth ground by the isolated power supply and isolated serial communications port.

2.4.2.1 DAS CPU, Opto-Isolators, and Control Logic

The DAS CPU and its associated control logic are responsible for the overall control and operation of the DAS. DAS CPU U1 is a single chip microcomputer (HD63B03Y) with onboard parallel and serial ports and 256 bytes of RAM.

The parallel ports are bidirectional. Initially configured as input on reset, each bit can later be configured as either an input or an output. The parallel ports of the DAS CPU are used to control the ECG lead switching, ECG fast charge, multiplexer channel selection, IBP channel testing, and the temperature channel switching. Additionally, inputs from the various power supplies are monitored for power supply faults. ADC interrupts, status information, and ADC calibration control are also handled through the parallel ports. Refer to 2.4.2.8 for a full definition of the parallel port assignments.

Communications with the Monitor system processor is through the serial communications port, paragraph 2.4.2.8. Isolation for the IO channels is provided by opto-isolators U5 and U6. Q9 supplies the LED current for the transmit opto-isolator.

Control logic U3 and U4 provide for DAS CPU address space mapping and communications baud rate clock generation. Both the address line A15 and the DAS CPU E clock must be high to enable EPROM U2; thus, the EPROM is addressed from 8000 hex through FFFF hex. Test point TP1, if grounded, disables the onboard EPROM, thereby allowing an external memory to access the bus from the same address space. In the ADC mapping logic, address line A15 must be low and address line A14 must be high to select the ADC. Thus the ADC is mapped at addresses 4000 hex through 7FFF hex. The DAS CPU E clock is added to deglitch the output.

U4 is a standard D type flip-flop configured as a divide-by-two counter. The DAS CPU E clock is divided from 2 MHz to 1 MHz by this circuit. The output of the clock generator is applied to the external baud rate clock input of the DAS CPU. The DAS CPU uses this as a 16X baud rate clock, giving a serial data rate of 62.5 K baud.

On power up, or if the digital supply ever goes out of tolerance, reset generator U16 will cause a DAS CPU reset. Once proper operating conditions are detected, the reset is removed after a pre set delay. A reset can be generated manually by grounding RESET IN test point TP9.

2.4.2.2 Analog to Digital Converter and Multiplexer

Analog-to-digital converter U7 has a resolution of 12 bits plus sign and has an onboard sample and hold amplifier. Other features of the ADC include automatic calibration and automatic zeroing of the input. In the 8700 DAS all conversions are done with an auto zero cycle. To ensure conversion accuracy over temperature, an auto calibration cycle is executed once for each pass through the MUX channels. The ADC presents the 13-bit data in two bytes, high byte first and sign extended.

The ADC clock source is the 2 MHz DAS CPU E clock. For each conversion, the ADC requires 26 clock cycles to execute an auto zero, seven cycles to acquire the signal, and 27 cycles to convert the sample. This results in an overall conversion time of 30 microseconds.

To protect the ADC input from overvoltage, a clamping network is used between multiplexer U9 and buffer amp U29. Series resistor R1 protects the ADC input from overcurrent should the buffer output go high for any reason.

The reference voltage for the ADC comes from +5V linear regulator U12. Since ratiometric techniques are used for all precision measurements in the DAS, the absolute value of the ADC reference voltage is not critical. An error output signals the DAS CPU if a fault is detected in the ADC reference.

U9 is a standard eight-channel single-ended analog multiplexer. The desired signal is selected by the MUX control lines MUX0 through MUX2. Multiplexer channel assignments are listed in paragraph 2.4.2.8.

2.4.2.3 ECG Channel and Lead Switching

The ECG channel consists of an input protection network, lead switch circuit, instrumentation amplifier (IA), lead fail detection circuits, common mode nulling loop, high-pass filter with a fast charge setting, and a fourth-order low pass filter. Display channel gain is 800 with a bandwidth of .05 to 40 Hz.

The input protection network consists of high voltage series resistors, neon surge suppressors, high value series resistors, filter capacitors, and slew leakage diodes. The neon surge suppressors protect the input from defibrillator voltages by turning on at 60 to 90 volts. The power resistors limit the amount of defibrillator energy lost to the monitor. A resistor is placed in series with the ECG shield terminal to limit currents induced in the ground plane during defibrillation. The high value series resistors, in concert with the filter capacitors, form a passive low pass filter to reduce electro-surgical noise. The last stage of protection is the back-to-back diodes, which limit the voltage appearing at that point to a bit more than 5V.

The lead switch circuit provides a means for switching among the three standard ECG lead configurations. Signal gating is performed by quad single pole single throw analog switch U14. The DAS CPU controls the lead configuration with its four lead select lines LS0 through LS3. The outputs of the analog switches are connected to either the plus or the minus inputs of IA U13 and also to the inputs to the lead fail and common mode nulling loop. Using the four lead select lines, all standard lead configurations can be realized. Refer to paragaph 2.4.2.8 for the lead switching bit combinations.

The Instrumentation amplifier (IA) amplifies the differential signal presented by the lead switch and converts it to a single-ended signal. The differential gain of the IA is set to 10. The IA input signals are buffered and sent to the common mode nulling circuit, where they are summed, inverted, filtered, and amplified. The resulting signal is then routed to the third patient connection, closing the loop. The loop drives the sum at the input of inverter U19-9 to zero, thereby nulling the common mode voltage at the patient signal connections. Loop gain is 409 with a bandwidth (set by C41 and R45) of 42Hz. To compensate the loop, R45 and C41 form a zero which cancels the pole formed by the driven lead's input resistor feeding the signal leads' input resistors and filter capacitors.

With the common mode nulling loop closed and both signal leads connected, all leads will be at near ground potential. When a lead fail occurs, high value pull-up resistors at the inputs of the individual lead buffer amps pull up the open signal input(s) well above any expected value. The buffered IA input signals are routed to individual channels on the multiplexer, where they can be monitored for the "lead off" condition.

The IA is connected to give an inverted version of the differential input voltage. The IA output is fed to an inverting high-pass filter (containing part of U10) having a gain of 20. The time constant of this filter is normally three seconds, to give a cutoff frequency of .05 Hz. Following a lead switch, or if the baseline is found to to be too far from zero, the time constant of the filter may be shortened by bringing FCHG-0 low. Baseline can be quickly reestablished in this way.

Low Pass filtering is performed by a fourth order, 40 Hz Butterworth VCVS low pass filter comprised of two gain-of-two stages. Because the IA and the high pass filter have high gain and wide bandwidth, the first stage of the low pass filter has been placed between them to minimize the chance of oscillation due to stray coupling from the high pass filter output back to the IA input.

2.4.2.4 Invasive Pressure Channels

The transducer is a standard resistive bridge blood pressure transducer with a sensitivity of 5 ~uV/V/mmHg. Excitation for the transducer is a buffered copy of the ADC reference. Thus the transducer output is 25 ~uV/mmHg. Since the excitation voltage and the ADC's reference are nearly the same, the system is ratiometric and variations in the excitation tend to cancel out.

The output of each transducer goes to two single pole double throw analog switches contained in U37. These switches allow test voltages to be applied to the input of the IBP channel for testing the channel gain and offset. The microprocessor may at any time switch the channel input to the reference network to measure the gain and offset of the entire channel to within 1%.

Depending on the state of the IBP test control lines (Port 6, paragraph 2.4.2.8) the reference network applies either a test voltage, or ground, to the IA input. A seperate network exists for each channel. The test voltage for a given channel is derived from its own excitation output, thereby giving a check of the health of the excitation buffer.

The output of the test switches feeds an instrumentation amplifier (U30 and U31) which amplifies the differential signal from the transducer (or reference network) and converts it to a single-ended signal. The gain of the IA is set to 100. The IA also minimizes the amount of common mode noise voltage that will be amplified and enter the measurement system. The output signal from the IA is then presented to the low pass filter.

A low pass filter similar to that used in the ECG section bandlimits the amplified signal to 40 Hz, and further amplifies the signal with a gain of 4. The low pass filter then presents the signal to the ADC for conversion to digital values. The total gain of the channel is 400; therefore, for each torr of pressure at the transducer, the voltage at the ADC is 10 mV. Since the ADC resolves 1.2 mV per LSB, each millimeter of mercury represents 8.3 LSBs, and each LSB represents .12 mmHg.

2.4.2.5 Temperature Channel

The temperature circuit determines the patient temperature by precisely measuring the ratio of the temperature probe resistance (YSI 400 series) to that of precision reference resistor R41. This is accomplished by use of the voltage divider relationship between R41 and the temperature dependant resistance of the transducer.

The current in the probe is low to to limit self heating. The gain of the amplifier is set only low enough that a cold probe at the 8700's minimum expected ambient temperature can be detected when plugged in.

DC excitation current is supplied via R39 to the top of the voltage divider. The excitation voltage, VX is gated to a gain stage by an analog switch when the gate excitation control signal GEX is low. Similarly, the voltage appearing across the temperature transducer (VT) is gated to the gain stage by asserting (active low) gate transducer control signal GTR.

The offset voltage of the gain stage is reduced as a source of error by measuring the offset voltage. The measured offset may then be subtracted in software from the subsequent measurements of VX and VT. Analog ground is gated to the input of the gain stage by asserting (active low) gate offset control signal GOF (Gate Offset).

RF rejection is provided by a passive LC filter consisting of an inductor and 2 capacitors. Further filtering is done by the RC filter in the VT tap.

Self-test capability is provided by energizing relay K1, replacing the temperature transducer with precision self-test resistor R42. The resistor is equivalent to a transducer temperature of 37.1 °C. The relay is activated by gate reference control signal GRF being asserted (active low). A level shifting network allows the use of the negative supply voltage for energizing the relay.

2.4.2.6 Isolated Power Supply

The isolated power supply, in conjunction with the isolated serial communications port, provides patient isolation from earth ground. It consists of a medical grade isolated DC-DC converter and several linear voltage regulators. Additionally, a power-on reset curcuit resets the DAS when power is stable.

Isolated DC-DC converter PM1 takes the 12 volts supplied by the non-isolated supply and provides isolated, unregulated +/- 12 VDC outputs. A shutdown input is provided that allows the Monitor system DAS CPU to interrupt power to the DC-DC converter, thereby reducing power consumption if the DAS is not being used.

The +5 volt logic supply is provided by a linear voltage regulator, U18. This voltage is monitored by reset circuit U16. A reset is generated whenever the +5 volt supply is below 4.5 volts. The regulator also has an open collector error output that signals when the regulator output is more than 5% out of the specified +5 volt limit, or when the internal current limit or thermal limit is in operation. This output is monitored by the DAS CPU at the PWROK input (P57, paragraph 2.4.2.8).

The +9 volt supply (U15) is provided by the same type regulator as is used for the logic supply. Its error output is also connected to PWROK (paragraph 2.4.2.8) to be monitored by the DAS CPU.

The IC used for -9 volt supply U17 has no error output, and an unused analog switch in the temperature circuit is dedicated to measuring it. The supply voltage is resistively divided at the switch input to produce a nominal -1.59 volt signal at the ADC.

The +5 volt ADC supply (ADC5V) is used only by the ADC. Regulator IC U12 is the same as that used in the +5 volt supply. The error output (VRFOK) is monitored by the DAS CPU.

The -5 volt supply is used only by the ADC. Regulator IC U25 is the same as that used in the -9 volt supply. This supply is divided by two and applied to the MUX to be monitored by the ADC.

Schottky diodes CR9, CR16, CR17, and CR18 are used with the voltage regulators to protect against latching during power up.

2.4.2.7 Addressing

ROM $8000 thru $FFFF
ADC $7000 "ADCCS-0"
ADC MSbyte is at $7000 and the LSbyte is at $7001.

2.4.2.8 Port Assignments

All ports are bidirectional, initially configured as inputs. Input/output status is given in parentheses.

P20 (o) => GRF control for temperature channel. Setting this output to zero connects a 1.35 K ohm, +/- .05% reference resistor to the input.

P21 (o) => GOF control for temperature channel. When set to zero, the temperature switch (U27) connects the input of the temperature channel gain stage to ground. This should be break before make with P25, P26, and P60.

P22 (i) => Baud rate clock input. The signal presented to this input is the E clock of the microprocessor divided by 2.

P23 (i) => Receive data input for serial port.

P24 (o) => Transmit data output for serial port.

P25 (o) => GTR control for temperature channel. This is an output which connects the temperature probe to the input of the temperature channel gain stage when set to 0. This should be break before make with P21, P26, and P60.

P26 (o) => GEX control for temperature channel. This is an output that connects the temperature channel excitation voltage to the input of the temperature channel gain stage when set to 0. This should be break before make with P21, P25, and P60.

P27 (o) => ADCCAL-0: CAL control for the ADC. This bit is programmed as an output. It is active low (O = ADC CAL mode). CAL should be toggled with the ADC deselected. EOC will go low while the ADC is calibrating, and return high upon completion of the calibration process. Power on reset initiates an ADC calibration, however this is not guaranteed to produce valid results. After power on, wait till EOC is high, then initiate an ADC calibration.

P50 (i) => ADCIRQ: ADC interrupt input.

ECG Lead select table	Lead
LEAD SETTING	I II III
P51 (o) => LS0 - ECG lead select	0 0 1
P52 (o) => LS1 - ECG lead select	0 1 1
P53 (o) => LS2 - ECG lead select	1 0 0
P54 (o) => LS3 - ECG lead select	1 1 0

Use "break before make" when switching leads. To open all inputs, set LS0,1,2, & 3 high

NOTE: P53 is initially set as a "HALT" input. A pullup is required to force the input into a safe state until it can be programmed.

P55 => EOC input from the ADC. This bit reflects the status of the ADC EOC output. EOC is low during calibration or conversion.

P56 (i) => VRFOK: ADC reference status input. When low this input indicates that the ADC5V regulator has an error condition.

P57 (i) => PWROK: Power supply status input. When low this input indicates an error condition is present in the +5V or +9V power supplies.

P60 (o) => GN9V-0: Gate Negative Nine Volts output, used during self test to determine the value of the negative nine volt supply. This should be break before make with P21, P25, and P26.

P61 (o) => IBPTZERO-0: IBP Test Zero when low output. When either IBP channel is in test mode (either IBPT1 or IBPT2 is low), bringing this output low allows input offset to be measured.

P62 (o) => IBPT1-0: IBP Test channel 1 when low - Puts IBP channel 1 into self test mode.

P63 (o) => IBPT2-0: IBP Test channel 2 when low - Puts IBP channel 2 into self test mode.

IBP test mode table

Channel1	Channel2	P61	P62	P63
transducer	transducer	X	1	1
transducer	meas offset	0	1	0
transducer	meas gain	1	1	0
meas offset	transducer	0	0	1
meas gain	transducer	1	0	1
meas offset	meas offset	0	0	0
meas gain	meas gain	1	0	0

P64 (o) => FCHG-0 Fast CHarge when low - Bring this output low to quickly establish an ECG baseline.

P65 (o) => Multiplexer address line 0 (MUX0)

P66 (o) => Multiplexer address line 1 (MUX1)

P67 (o) => Multiplexer address line 2 (MUX2)

ADC Multiplexer channel assignments

Ch0 ECG

Ch1 Lead Fail +

Ch2 Lead Fail -

Ch3 IBP channel 1

Ch4 IBP channel 2

Ch5 Temperature channel

Ch6 Negative 5 volt power supply divided by 2

Ch7 Analog ground

2.4.2.9 A/D Converter

On power up, the ADC performs an auto calibration cycle. This procedure will last approximately 1399 clock cycles after power up, and although the results will not be valid, the cycle may not be interrupted.

An auto cal cycle may be started by bringing ADCCAL-0 low for at least 200ns, with ADCCS-0 high. EOC, which is initially high, should go low at the leading edge of ADCCAL, and should remain low for 1399 clock cycles.

A conversion is started by bringing ADCCS-0 and WR-0 low for at least 200ns. Auto zero begins with the rising edge of WR-0, and lasts 26 clock cycles. Acquisition occurs during the next 7 cycles. A falling edge on EOC signals the end of acquisition. The sampled input is converted over the next 27 clock cycles. End of conversion is signaled by the falling edge of ADCIRQ. Data may be read at any time after ADCINT goes low.

2.4.3 Analog Board

The analog board circuits are shown on schematic SC315-334 contained in Section 4. The analog board is the interface between the Monitor system processor and the Pulse Oximeter sensor and NIBP cuff sense hose. Additionally, the -12 volt power supply is located on this board.

The Pulse Oximeter section of the board provides adjustable amplitude AC drive current for the oximeter sensor's LEDs, amplifies the photo-current from the sensor photo-diode, demodulates and filters the detected signal, and amplifies the pulse component for conversion by the system processor A/D converter.

The NIBP section provides excitation voltage or current for the pressure transducer, amplifies the pressure transducer signal, and separates, amplifies, and filters the pulse component of the pressure signal. The transducer excitation is adjustable by the system processor for scale calibration. The offset of the transducer amplifier is adjustable by the system processor for auto-zero.

2.4.3.1 Control Interface and DAC

Addressable latches U21 and U22 provide 16 independently controllable static logic signals. The system processor performs the following sequence to program an output bit:

1. The desired logic level is applied to LATCHDATA (J1-32).

2. The address of the output bit to be programmed is applied to CHSEL<2:0> (J1-33,34,35).

3. The appropriate strobe signal (J1-30 or J1-31) (normally high) is pulsed low.

Quad 8 bit DAC U20 provides independently controllable voltages for pressure transducer excitation (SDAC, U20-19), pressure transducer offset (ZDAC, U20-20), and each oximeter channel (U20-1,2). To set an analog value, the channel is selected by CHSEL<1:0> (J1-34,35), the desired data are applied to PD<7:0> (J1-22 through 29), and DACSTB-0 (J1-36) (normally high) is pulsed low.

The reference voltage for the DAC is provided by U13. The output circuit of U13 is source-only. CR104, C52, and R98 are provided to sink current spikes originating from the reference input of the DAC at certain code transitions.

The -5 volt supply for the DAC is provided by U14.

2.4.3.2 Clock Generator and Sync

The master clock for the analog board functions is a nominal 115kHz signal provided by the system processor (BCLK115K, J1-20). This is used to generate the clocks for the isolated power supply and -12 volt power supply and for the pulse oximeter LED drive and synchronous detectors. The actual frequency is 16 MHz divided by 139, or 115.108 kHz.

The input clock is first divided by 2 by one section of U15. The complementary outputs of U15 are supplied to U35 for the isolated power supply. One output (M12CLK) is provided to R114 for the -12 volt supply. M12CLK is also applied to the clock inputs of presettable binary counters U16 and U34.

U16 provides the carrier-frequency reference clocks for the pulse oximeter synchronous detectors. These two clocks, nominally 14.4 kHz and 7.2 kHz, are provided (with their complements derived by inverters U18) to the synchronous detector switch U17.

U16 generates a carry pulse during the time it is in state 15 (1111 binary). This pulse (SYNC) is coupled through opto-isolator U1 to the load input of an identical counter U6 in the isolated section. This pulse forces U6 to be counting in step with U16, maintaining the correct phase relationships between the LED drive signals and the synchronous detector clocks.

U16, U34, and U7 work together to provide an isolated 4 bit control word in the isolated section (used for LED intensity control and sensor decoding.) SYNC from U16 is provided (inverted) to the load input of U34. When U16 switches between state 15 and 0, its carry output is asserted, asserting the load input on U34. This forces U34 to assume the state selected by its preset inputs. Since U34 is clocked at the same frequency as U16, its count will be offset from the count of U16 by a number of clock pulses determined by the setting on the preset inputs. The carry output of U34 (DSYNC) is coupled through opto-isolator U2 to the load input of U7 (a counter, but used as a 4 bit latch) in the isolated section. U7 latches the state of counter U6 (which is the same as U16) at the time DSYNC is asserted.

2.4.3.3 Negative 12 Volt Power Supply

The -12 volt supply is a conventional pulse width modulated flyback switching topology operating at about 57.5 kHz. A rectangular pulse of a controlled duty cycle is provided to the base of Q12. When Q12 is on, the current in L1 increases linearly at a rate proportional to V / L. When Q12 is subsequently switched off, the current in L1 continues to flow, and finds an alternate path through CR7, charging the output capacitors (C14, C6, C8, and C57) to a negative voltage. The duty cycle determines the output voltage; a higher the duty cycle results in a higher (more negative) output voltage.

The duty cycle is controlled by quad comparator U28 and associated circuits. The four outputs are wire-ANDed to driver transistor Q15, so any one of the 4 comparators can turn OFF the output transistor Q12. Thus, Q12 is ON only when all four comparators agree that it is appropriate. The comparators provide functions of current limiting, clock failure protection, and voltage regulation.

The 57.5 kHz clock (M12CLK) is coupled through R114 to C53. This network approximately integrates the square wave, generating a roughly triangular wave of about 2 volts p-p at U28-6,9. This triangular wave is attenuated by R118 and R119, providing a roughly triangular wave of about 0.37 volts p-p at U28-10.

Voltage regulation is controlled by U28-10,11,13. The difference between the negative output voltage and +12 volts is compared with the low amplitude triangle wave at U28-10. When the supply is in regulation, the voltage at U28-11 is at a point between the maximum and minimum voltages of the triangle wave at U28-10, and the output U28-13 defines the duty cycle of the power supply. If the output voltage changes, the threshold moves to a different level on the triangle wave, selecting a higher or lower duty cycle as needed to correct the output voltage.

Current limiting is controlled by U28-2,4,5. The inductor current, and consequently the peak collector current in Q12, flows through R123, generating a proportional voltage at U28-4. If the current increases to the point where the sense voltage exceeds the reference voltage on U28-5, U28-2 will pull low and inhibit the drive to Q15. Hysteresis is provided by positive feedback via R121, so the current must decay below the threshold for the supply to be re-enabled. In the event of an overload, this comparator will cycle on and off, limiting the Q12 collector current and the output current to a safe value. The current limit also operates at turnon until the output capacitors are charged.

Clock failure protection is provided by U28-8,9,14 and U28-1,6,7. If the clock input is at the correct frequency, the triangle wave at U28-6 will never be higher than the reference voltage at U28-7 nor lower than the reference voltage at U28-8. This normal condition results in these two comparators allowing Q15 and Q12 to turn on. If the clock input stops in a low state, U28-14 will pull low; if the clock input stops in a high state, U28-1 will pull low. Either of these conditions will inhibit the drive to Q15, turning off the supply.

The ripple voltage at Q12-E is of opposite phase with the output ripple voltage that is due to the equivalent series resistance (ESR) of the output filter capacitors. C15 couples this voltage to the output to reduce the ripple voltage on the -12 volt supply.

2.4.3.4 Isolated Power Supply

Power is supplied to the isolated pulse oximeter sensor interface circuitry by a conventional push-pull switching power supply. The two halves of the primary of T3, a ferrite pot core transformer, are alternately grounded by Q13 and Q6, generating a square wave across the center tapped secondary. This square wave is full wave rectified by CR4 and CR5. The resulting DC voltage is filtered by C4.

The square wave provides the clock, via R6, to the clock input of the counters U6 and U7.

CR8 half wave rectifies the square wave to generate a low current -5 volt bias supply for the photo-diode. The -5 volt supply is regulated by R19 and zener diode CR9, and filtered by C13.

Quad comparator U35 provides the gate drive voltage for Q6 and Q13, and senses any over-current condition. U15 controls the current limit and on/off functions.

Comparators U35-8,9,14 and U35-2,4,5 amplify the complementary 57.5 kHz clock signals from U15-5,6 to approximately 12 volts, ensuring the FETs are adequately turned on. The outputs of these comparators will both be low, turning both transistors off, if U15 is reset (U15-8 high).

In normal operation, the on/off control signal from control latch U21-12 is clocked through U15 to enable or disable the drive to the transistors.

Supply input current flows through R132, generating a voltage proportional to the input current. In the case of excess current load, this voltage exceeds the threshold set by R130 and R131. U35-1 then pulls low, resetting flip-flop U15, thereby disabling the drive to the transistors and turning off the supply. When the load current decays, the supply will be turned on at the next clock cycle. In the event of a continuous overload, or during turn-on, U15 will be reset before the completion of each half-cycle, thereby limiting the current to a safe value.

2.4.3.5 LED Current Control

The two LEDs in the oximeter sensor are driven by square wave current pulses at 7.2 kHz and 14.4 kHz. The current is adjustable to 16 levels from zero to 60 mA peak. The operation of the RED driver is described; the IR driver operates similarly.

Resistor network R10, R11, R20, R21, and R22 comprise a 4 bit D/A converter driven by data latch U7, described elsewhere. The non-inverting inputs of dual op-amp U8 are driven by the adjustable 0-1 volt D/A output. U8 integrates the difference between the average voltage across sense resistor R55 and the control voltage. U8-1 drives the base of Q10 to force the average voltage across R55 to equal the D/A voltage, thereby controlling the average LED current.

Diodes CR100 and CR101 allow Q10 to be turned off when U6-13 is low. The base of Q10 is thereby driven by a square wave of the appropriate amplitude to cause the average voltage at Q10-E to equal the D/A voltage. Since Q10 is off for half of the time, the peak current will be twice the average current.

The value of R55 was chosen to establish a peak current of 60 mA when the D/A voltage is 1 volt.

2.4.3.6 Sensor Code Detection

Each sensor contains a resistor that connects from the CODER input (J2-4) to isolated ground. The divider formed by R135 and the coding resistor establish a voltage at U36-2 that is a function of the coding resistor.

U36 is an 8 bit A/D converter with serial data output. The operation is controlled by two of the programmable output bits from U7. The serial data output is coupled to the system processor connector by opto-isolator U3. Q14 buffers the output from the A/D converter to allow it drive the opto-isolator LED.

Since the same control bits to the A/D converter are used to vary the LED intensity, oximeter operation must be suspended when accessing the A/D.

2.4.3.7 Sensor AC Amplifiers

The photo-current from the sensor photodiode flows through the primaries of tuned transformers T1 and T2. T1 is resonant at 14.4 kHz and T2 is resonant at 7.2 kHz. R18 and R5 set the Q of the resonant circuits. The AC voltage appearing across the secondary of T1 or T2 is proportional to the illumination received by the photo-diode from the LED excited by the corresponding frequency.

The RED LED is driven at 14.4 kHz, and its light results in the voltage across T1. The IR LED is driven at 7.2 kHz, and its light results in the voltage across T2.

The following description is for the RED channel; the IR channel operates similarly. Dual op-amp U9 is configured as a variable gain noninverting amplifier. Gain is controlled by selecting among the different taps of the feedback resistor divider network. The selected tap is fed back via U11, an 8 input CMOS multiplexer controlled by RGAIN<2:0> from the control logic circuit. Gain can be varied from 1 to 128 in power-of-two steps.

The output of U9 drives a phase splitter amplifier composed of two sections of U10. The gain from U9 to U10-7 is +11 and the gain from U9 to U10-1 is -11. These complementary signals drive the synchronous detector.

Asserting the POPULSE-1 signal turns on Q7, applying a 50 mV step to U10-3. There is a gain of +12 from U10-3 to U10-1, and a gain of -10 from U10-3 to U10-7. This unbalanced signal into the synchronous detector causes a corresponding step at the output of the detector, which is used as a self-test of the gain and step response of the following signal processing circuitry.

R50 provides a fixed offset to ensure that the synchronous detector signal is always slightly positive with no AC signal input. The offset is subtracted by the processor during oximeter operation.

2.4.3.8 Synchronous Detectors and Filters

The light intensity information received by the photodiode is contained in the amplitude of the AC signals from the sensor AC amplifiers. This signal must be converted to a voltage proportional to its amplitude (AM demodulated) in order to be processed by the remainder of the analog system.

U17 comprises a synchronous demodulator. Since the phase of the incoming modulated AC signal is known, the demodulator selects either the signal or its complement (whichever is positive at the instant), thereby full-wave rectifying the signal. The full wave pulses are low-pass filtered by the two pole low pass filter (U19 and associated components). The output of the filter is the average value of the full wave rectified signal, and is proportional to the amplitude of the incoming AC signal.

The demodulated and filtered voltage is provided to the A/D converter (MRED and MIR) and to the pulse amplifiers.

2.3.4.9 PO Pulse Amplifiers

The pulsatile information in the incoming signal from the sensor is a small fraction of the total received signal, but its amplitude must be accurately measured by the processor system. The pulse amplifier provides the gain necessary to amplify the pulse component such that it can be measured with adequate resolution by the A/D converter.

Amplifying the combined constant and pulse components would result in over-ranging the A/D converter, so the majority of the constant component of the sensor signal is subtracted before the amplification. The D/A converter (U20) provides an adjustable offset that is set to bring the output of the pulse amplifier within the range of the A/D converter. The amplified pulse signals are provided to the system processor for A/D conversion (LRED and LIR).

2.4.3.10 Pressure Transducer Excitation

The NIBP section measures the cuff pressure using a silicon piezo-resistive strain gauge pressure sensor. The output voltage of the sensor is proportional to the product of the transducer excitation (voltage or current) and the air pressure at its measuring port. The excitation is provided by U25 and the current driver stage comprising Q1 and Q2. The magnitude of the excitation is controlled by the D/A converter, in order that the CPU can adjust the scale factor of the transducer system for automatic calibration.

The board is designed to accommodate four different transducers, with different excitation requirements. Current or voltage mode of excitation is selected by different configurations of resistors and jumpers.

Buffer amplifier U25-5,6,7 provides a voltage proportional to the excitation for use by the CPU as a self test.

2.4.3.11 Transducer Amplifier

U23, a low noise dual op-amp, is configured as a differential amplifier to amplify the output voltage of the transducer. The gain is adjusted to accommodate different types of transducers by use of different values for R99. The output of the amplifier (U23-7, PT) is provided to the system processor.

The transducer output includes an offset that must be subtracted for accurate pressure measurement. In operation, the pneumatic system can vent the transducer to atmosphere ("zero" gage pressure). The offset is then adjusted by the use of the D/A converter. The D/A output is scaled and buffered by U24-5,6,7.

R84 couples a test pulse signal, generated by asserting the signal FPTTST-0, into the pressure transducer signal path for self test and diagnostics.

2.4.3.12 BP Pulse Amplifier and Clamp

The pulse component (typically one percent) of the cuff pressure signal is separated from the cuff pressure signal by a two pole low pass filter (U24-12,13,14) and a two pole passive high pass filter. The pulse signal is amplified by U24-8,9,10. The gain is selectable between two values by the logic signal ADULT-0.

The blood pressure algorithm requires the ability to initialize the high pass filter in the process of separating and measuring the pulse signal. This function is provided by the two switches in CMOS switch U26 controlled by CLAMP1 and CLAMP2. When these switches are on, the output of the first section of the high pass filter, C42, is grounded, and the second is connected to a known reference voltage provided by R93 and R94.

2.4.4 Pneumatics Board

The pneumatics board circuits are shown on schematic SC315-376 contained in Section 4. Functionally, these circuits consist of the valve drive circuit, the pump drive circuit, the overpressure and safety interlocks, the time delay circuit, and the thermal switch circuit.

2.4.4.1 Valve Drive Circuit

The valve solenoids are powered by the +12VU supply and energized by digital control of VMOS FET switches Q8, Q3 and Q4. ZERO valve MT1 is energized when Q3 is turned on by ZERO. When energized, the ZERO valve blocks the CUFF input port and connects the pressure transducer to atmosphere. When deenergized, the ZERO valve connects the pressure transducer to the CUFF input port.

DUMP valve MT3 is energized when Q4 is turned on by U2-10. U2-10 goes high when DUMP-0 is asserted, or when the fail-safe alarm (FAILSAFE-0) or the overpressure signal (OP-1) is asserted from U3-3. When energized, the DUMP valve blocks the output of the air pump and ports the CUFF pressure port to atmosphere. When de-energized, the DUMP valve ports the output of the air pump to the CUFF pressure port.

DEFLATE valve MT2 is energized when Q8 is turned on by U2-4. This occurs either when DEFLATE-0 is unasserted, or when FAILSAFE-0 or OP-1 is asserted. When the DEFLATE valve is energized, the deflate line from the CUFF pressure port is blocked. When the DEFLATE valve is deenergized, the deflate line is ported to atmosphere. Zener diode D1 provides for a faster collapse of the solenoid fields of MT2 and MT3. R25, R26 and R27 provide VLVSENSE, an average voltage reading indicative of the current drain of all three solenoids that is used only in manufacturing tests.

2.4.4.2 Pump Drive Circuit

The +12VU supply is applied to the pump through Q2. When PUMP_ON is asserted (high) and the DEFLATE valve is energized (closed), the gate of Q1 is brought low by U2-11. Q1 and R11 invert the active-low signal from U2-11 to an active-high needed to turn on Q2.

Pump current is sensed by R14. Sense voltages representing currents greater than about 1 Amp, possibly indicating a locked roter or other pump fault, will trip comparator U4, triggering the time delay circuit. The delay allows pump turn-on transients to be passed without falsely signaling an overcurrent condition.

2.4.4.3 Overpressure Switch and Safety Interlocks

The overpressure switch is fed by a pneumatic line from the CUFF pressure port. The switch is set to trip at around 300 mmHg, triggering the time delay circuit. The delay allows pressure transients to be passed without falsely signaling an overpressure condition. The normally low comparator output of the time delay circuit holds the NOR latch (U3-8,9,10 and U3-11,12,13) into the reset state. With a sustained overpressure condition (set by the time delay circuit), U3-12 will be pulled high by R12, setting the NOR latch to assert OP-1.

OP-1 enables U3-3 to energize the DUMP valve and de-energize the DEFLATE valve to dump cuff pressure and turn off the pump (U2-12). OP-1 also turns on Q7, which provides a back-up to energize the DUMP valve in the event Q4 fails. The CPU reads the OP-1 signal as a digital input bit to generate an alarm. When the overpressure switch closes, the NOR latch may be reset by PNEURESET-1 at U3-8. C1 prevents a stuck PNEURESET-1 from holding the latch in the reset state.

The fail-safe alarm interlocks are effected by U3-3 which disables U2 when the fail-safe alarm occurs (FAILSAFE-0). Thus, a fail-safe alarm will cause the DUMP valve to energize, the DEFLATE valve to deenergize, and the pump drive circuit to be disabled.

2.4.4.4 Time Delay Circuit

The time delay circuit, formed around comparator U4-1, buffers the raw overcurrent or overpressure inputs to allow for transients. Pressure switch S1 (or alternate part S2) is normally open. The open collector overcurrent comparator U4-2 is normally high (open). As a result, C8 is normally uncharged. The voltage at the comparator input U4-6 is then equal to the +5V supply, well above the trip point set by voltage divider R4 and R13.

When either the switch or the comparator grounds the circuit input, C8 charges with a time constant set mainly by R6. Diode CR4 is reverse biased as the capacitor charges. Should the switch open before the comparator input voltage has reached the trip point, as happens with pump pressure or current transients, C8 will rapidly discharge through R8 and CR4, which may now be forward biased. If the overpressure or overcurrent condition persists, the trip point will be reached in about 100 milliseconds. Resistor R12 provides hysteresis to avoid oscillations near the trip point.

2.4.4.5 Thermal Switch Circuit

The thermal switch circuit turns on a cooling fan at 55°C, and provides an overtemperature indication when the temperature rises above 70°C. Thermister RT1 has a negative temperature coefficient of resistance. RT1 and R22 provide a temperature-dependent voltage input to comparators U4-13 and U4-14. The 55°C trip point is set by voltage divider R23/R24, and the 70°C trip point is set by voltage divider R30/R31. R29 and R20 provide hysteresis for the two comparators. C2 and C3 are used for noise rejection. When Q6 is switched on by U4-14, the return path from the +12 VDC supply is closed and the fan operates. The output from U4-13 is the HITEMP-0 signal to the system processor.

While the pump is operating, U4-8 is pulled down through CR6 and R21 to temporarily raise the fan control trip point beyond any expected temperature, resetting the comparator and turning off the fan.

2.4.5 Battery Switch Board

The battery switch board circuits are shown on schematic SC315-371 contained in Section 4. The battery switch board provides the following functions:

Connection of either of two batteries to the DCSOURCE common power bus.

Connection of either storage battery to a test load.

Coupling of an external DC power source (EXT_DC) to the common DCSOURCE power bus, including protection for overcurrent, overvoltage, and reversed input polarity.

Generate a voltage proportional to the EXT_DC voltage

Detection of the presence of the external ac power source.

A low power circuit to debounce and latch power supply control switches ON and OFF.

Connection of the regulated battery charger voltage to either of the two storage batteries.

2.4.5.1 Battery Switch Power Supply

Several power supply voltages are required for the operation of the battery switch board. VB, the diode coupling of BAT1+ and BAT2+ via CR13 and CR14, is used to generate MOSFET gate drive voltage. 18VBUS is also coupled to VB via CR16. The 18VBUS is reduced (Vz=5.1) by series reverse bias Zener diode CR25. VB and EXT_DC are diode coupled by CR18 and CR17 and regulated by R4 and 15 V Zener diode CR20, an MMBZ5245, to provide a power source for the power supply latch gates and a source for the MAX663 voltage regulator U4. U4 provides a +5V regulated output to power comparator U3, and generates a 2.5V reference using 33.2k ohm divider resistors R24 and R25.

An increased gate drive voltage is required to control the high side MOSFET devices used to switch the batteries to DCSOURCE, the battery charger, and the test load. Charge pump converter U1, an ICL7662, is used with rectifiers CR11 and CR12 and capacitors C9 and C13 to generate a voltage (VGATE) approximately twice that of the greatest battery voltage minus three diode drops.

VGATE is only generated when AC line voltage is connected, as indicated by the presence of 18VBUS, or when the unit is switched on (ON-0 asserted). VB is switched to U1 with Q16, which is driven on after either Q11 or Q12 is turned on. Q11 is connected to the switched +5V supply through R11. 18VBUS is connected to the base of Q12 through divider resistors R22 and R32.

2.4.5.2 Battery to DC Source Switch

The battery switch board includes two sets of digital logic controlled switches to connect either storage battery to the DC power bus (DCSOURCE). The positive terminal of battery one (BAT1+) is connected to the drain of IRFZ40 N Channel power MOSFET Q24. The source of Q24 is then connected through 1N5825 Schottkey rectifier CR2 to the DCSOURCE power bus. The gate of Q24 is connected to VGATE (typically, twice the maximum battery voltage minus 2 volts) through 33.2K ohm resistor R33, and to the collector of buffer NPN transistor Q15. With a logic low signal at USEBAT1-0, Q15 is off and Q24 turns on. If the potential at BAT1+ is greater than the other sources (EXT_DC or the other switched on battery) connected to DCSOURCE, then it will supply current to DCSOURCE. With a logic high signal at USEBAT1-0, Q15 turns on, pulling the gate of Q24 close to 0V and turning Q24 off. 15V Zener diode CR10 is connected between the gate and source of MOSFET Q24 to limit the Vgs of Q24. The forward voltage drop from BAT1+ to DCSOURCE is 0.8V at 3 Amps. The switch for battery two operates similarly.

2.4.5.3 Battery to Test Load Switch

Two sets of digital logic controlled switches connect either storage battery to test load resistor R1. The positive terminal of battery one (BAT1+) is connected to the drain of MTD5N05 N channel power MOSFET Q18. The source of Q18 is then connected through MBR140 rectifier CR6 to R1. The gate of Q18 is connected to VGATE through 100K ohm resistor R47, and to the collector of buffer transistor Q5. With a logic low signal (or open circuit) at TSTBAT1, Q6 turns off and Q5 turns on, pulling the gate of Q18 close to 0V and turning Q18 off. With a high logic signal at TSTBAT1, Q6 turns on, Q5 turns off, and Q18 turns on, connecting BAT1 to the test load. 15V Zener diode CR9 is connected between the gate and source of MOSFET Q18 to limit the Vgs of Q18. The switch for battery two operates similarly.

The 49 ohm test load resistor R1 draws approximately 250 mA at 12 volts, similar to the typical pump current. Resistors R39 and R19 divide the voltage across R1 and provide BATTEST at J1-27.

2.4.5.4 External Power Sources

A source of external DC power can be connected to the battery switch board through connector J2. The external DC power is coupled to the DCSOURCE power bus by OR gate CR4. F1 provides overcurrent protection. Overvoltage and reverse polarity protection are provided by a crowbar circuit consisting of Triac Q27, Zener diode (Vz= 33 nominal) CR22, and resistor R2. External DC power is coupled to the battery switch power supply by CR17. A voltage proportional to EXT_DC, divided by 7.02 using R23 and R52, is available at J1-9.

2.4.5.5 18V Bus Detector

A logic level output AC_OFF at J1-4 indicates if 18VBUS is present. 18VBUS is divided by five by R53 and R58. U3-2,4,5, an LP339, compares this value to the 2.5V reference. R59 adds hysteresis and R18 pulls the open collector LP339 output to the +5V rail. The output is asserted (logic low) when external dc is less than 12.5 volts.

2.4.5.6 Power Supply Control Latch

Two sections of CMOS NAND gate U2, a 14093, are cross coupled to create a latch for the power supply OFF/ON control. Low true inputs at J1-2 and at J1-1 clear (OFF-0) and set (ON-0) the latch. The inputs are each pulled up with 33.2k ohm resistors R27 and R30. ON-0 is coupled to return with 0.01uF capacitor C1, but OFF-0 is coupled to return with a larger 0.1uF capacitor C6 to assure the latch is cleared on initial application of power. Rectifier CR19 rapidly discharges C6 when power is removed. R5 and R6 limit current through ON-0 and OFF-0. The outputs of this cross-coupled latch are inverted by the two remaining sections of U2 so the outputs are negated when both inputs ON-0 and OFF-0 are asserted. Latch output Q-0 from U2-10 is connected to SHutDowN pin 5 of MAX663 regulator U4. This allows the battery switch board regulated +5V supply to function only when the unit is on. Latch output Q from U2-11 provides a low true power supply_SHUTDOWN-0 signal at J1-8.

2.4.5.7 Battery Charger Controller

Off-board battery charge voltage is controlled by a voltage regulator, power switch circuit, and state machine logic. The operational sequence is:

STATE 1 - Connect VBC to BATT1+ until CHARGED-1 is true

STATE 2 - Connect VBC to BATT2+ until CHARGED-1 is true

STATE 3 - Wait for five minutes, then go to STATE 1

The regulator circuit consists of 100 ohm resistor R3 and Zener diode CR21, which assures the power rail for CMOS state machine logic devices does not exceed 15 volts. The input to this regulator (VBS) is only active when 18VBUS is powered, or when the unit is on.

The state machine operates under the control of a single input, CHARGED-1. A high true reset pulse on power up is generated by R28, C2, and Schmitt trigger NAND gate U8-11, 12, 13, a 14093. This pulse, with two additional sections of U8, clears 14020 delay counter U6, and directly sets one half of 14017 D flip flop U9A.

Timer ICM7555 provides a 0.85 Hz, 1.17 second period, approximately 50% square wave to clock the flip flops and delay timer U6. Flip flop U9B, 14093 NAND U8-1,2,3, C17, and R60 form a one-shot driven by the timer output, the output of flip flop U9A, and the level of CHARGED-1. The output of U9B pulses high to clock the 14017 counter decoder whenever CHARGED-1 goes high with U9A Q-0 high, or when U9A Q-0 is driven low by 14020 counting to 256. Q2 or Q3 drive the battery charger output switching circuit VBC to BATT1+ or BATT2+. Q3 enables delay counter 14020.

Two sets of digital logic controlled switches connect the battery charger output to the positive terminal to either storage battery. The charger output VBC is connected to the drain of N channel power MOSFET MTD5N05 Q17. The source of Q17 is then connected through rectifier MBR140 CR5 to BATT1+. The gate of Q17 is connected to VGATE through 100K resistor R45, and to the collector of buffer transistor Q4. The base of Q4 is connected to state machine output CG1. With CG1 low, Q4 turns on, pulling the gate of Q17 close to 0 volts and turning Q17 off. With a high logic signal at DG1, Q4 turns off and Q17 turns on, connecting VBC to BAT1+. 15V Zener diode CR1 is connected between the gate and source of MOSFET Q17 to limit the Vgs of Q17. The switch for battery two operates similarly.

2.4.5.8 Connector Signal Description

Battery switch board connector signals include the following:

ON-0 (J1-1) Low true digital input from front panel momentary contact switches to power supply control latch. Sets latch when asserted.

OFF-0 (J1-2) Low true digital input from front panel momentary contact switches to power supply control latch. Clears latch when asserted.

USEBAT1-0 (J1-3) Low true, digital input, connects battery 1 to DCSOURCE when asserted.

AC_OFF (J1-4) Digital output, high true signal that detects whether the 18VBUS is greater than 12.5 volts, indicating that ac power is connected to the Monitor.

DCRET (J1-5,6) Return path for DCSOURCE, EXT_DC, and all control signals. Common with BAT_GND.

CHARGED-1 (J1-7) High true logic indicating that battery charger current is less than 50 mA. When asserted, the battery charge switch control is advanced to the next state.

PS_SHUTDOWN-0 (J1-8) Digital output, low true signal to disable the secondary (regulated output) portion of the power supply.

ZEXT_DC (J1-9) divided down EXT_DC power bus.

18V_BUS (J1-10) Intermediate, unregulated power bus from the system power supply.

DCSOURCE (J1-11,12,13,14) DC power source to the secondary (regulated output) portion of the system power supply.

BAT_RET (J1-15,16) Return path for BAT1 and BAT2. Common with DCRET.

BAT2+ (J1-20,22) Positive terminal of battery 2.

USEBAT2-0 (J1-21) Low true, digital input, connects battery 2 to DCSOURCE when asserted.

TSTBAT2 (J1-23) High true digital input, connects battery 2 to the test load when asserted.

BAT1+ (J1-24,26) Positive terminal of battery 1.

TSTBAT1 (J1-25) High true digital input, connects battery 1 to the test load when asserted.

EXT_DC- (J2-1) Negative lead of external DC source.

EXT_DC+ (J2-2) Positive lead of external DC source.

2.4.6 Power Supply Board

The power supply board, shown on schematic SC315-367 contained in Section 4, supplies regulated voltages to operate all the Monitor circuits. This module converts power from internal storage batteries, AC power line input, or an external DC source into the required regulated voltages for the monitor. Additionally, this module converts AC input power into a suitably regulated voltage and current for charging the internal batteries. Logic circuits are provided to signal the system processor when power is about to fail, so that the processor can shut down Monitor operation in an orderly manner.

2.4.6.1 Low Voltage Converter

The low voltage converter provides regulated +5 volts and +12 volts to the Monitor electronic circuits. Input power for the LV converter is a DC voltage of 10 to 32 volts, which is supplied by the monitor's batteries, external DC source, or AC line input via the line power converter. The LV converter is a pulse-width-modulated current-mode push-pull forward converter. The DC input voltage is supplied to the center tap of the primary of T4 from the DC source input or from the line power converter via diode CR10. Diodes in series with the DC source input to the power supply board isolate the DC sources from the line power converter when line power is available. The input voltage is alternately switched to the two halves of the primary of T4 by FETs Q11 and Q12, controlled by regulator IC U3. Two secondaries on T4 provide separate outputs for the +5 and +12 volt supplies. The square waves from two secondaries of T4 are rectified by diodes CR16, CR17, CR18, and CR19, and filtered by coupled inductor L4 and capacitors C29, C30, and C31. The +12 output is provided to the Monitor via J1-3 and its associated pins.

The gate drive for switching transistors Q11 and Q12 is provided by monolithic current mode regulator IC U3. The instantaneous input current into T4 is sensed by R34, which provides a voltage proportional to the input current to U3. The duty cycle of the gate drive signals is adjusted by U3 to maintain a correct input current into T4. The correct value of the input current is, in turn, determined in U3 by comparing an internal reference voltage with a voltage proportional to the 12 volt output provided by feedback network R21, R22, and R23. R22 is adjusted to set the +12 volt output to the correct value. The frequency of the gate drive signals is generated by an oscillator in U3 whose frequency is set by R30 and C25. Q15 buffers the oscillator signal across C25. This signal is combined with the current feedback signal from R34 to improve stability at low input voltages.

The output current of the 12 volt supply flows through R40 and R41, generating a voltage proportional to the current that is compared to the reference voltage by comparator U2-2, 4, 5. The 5 volt supply current is similarly compared by U2-13, 10, 11. The outputs of these two comparators are wire ORed to the current limit input U3-1. If the load current reaches an unsafe value, the supply will be shut-down. R25 and R26 set the maximum peak current into T4, while C24 provides a soft-start turn on characteristic for the supply. The output from the pulse width modulator regulator at C29 is nominally 5.5 volts. This voltage is regulated to +5 volts for delivery to other Monitor components by the 5 volt regulator comprised of Q13, U4, and associated parts. The 5 volt output is divided down to nominally 2.5 volts by R44, R45, and R46. This voltage is compared to a 2.5 volt reference in U4, which generates a gate voltage on Q13 to regulate the output to 5 volts. R46 is adjusted to set the 5 volt output to the correct value.

Under normal operation, the control circuitry is powered by the regulated 12 volt output via CR12. Q10 provides a regulated +9 volts to power the converter and control logic circuitry when the supply is in the standby (shut down) state.

2.4.6.2 Line Power Converter

The line power converter provides a nominal +18 volts DC that can supply the low voltage converter and the battery charger inputs. Input to the line power converter is 88 to 264 volts ac, 47 to 440 Hz, allowing the Monitor to operate on commercial AC power available throughout the world. This supply operates whenever AC power is present, and can operate the battery charger whether the Monitor is switched on or off.

AC input power arrives at the board via J2 and is full-wave rectified by BR1. The resulting DC voltage (120 - 370 volts DC) is filtered by C2 and C3. The tap between C2 and C3 provides a reference of one half of the total DC input voltage for the primary of T1. The power converter is a half-bridge, pulse-width-modulated forward converter. Transistors Q2 and Q3 are alternately switched on with equal variable-width pulses at a frequency of 150 to 200 kHz, applying equal positive and negative polarity pulses to the primary of T1. Diodes CR8 and CR9 rectify the pulses from the secondary of T1. The diode output is a train of pulses with an average voltage of 18 volts. The pulses are filtered by L3 and C12 to generate the 18 volt DC output.

The auxiliary secondary winding of T1 provides power (nominally 14 volts) for the regulator circuitry via rectifier and filter CR3, CR4, CR5, CR6, L8, and C9 and provides a feedback signal for the voltage regulator. Since this voltage is not available until the converter is operating, and is required for the converter to operate, a separate startup supply is provided.

Q1 and CR1 comprise a linear regulator providing nominally 10 to 12 volts when AC power is first applied to the input. When the converter begins operating, the gate to source voltage on Q1 is reduced, turning off Q1 and allowing the 14 volt supply to assume the auxiliary load.

The output voltage is regulated by monolithic IC regulator U1. An oscillator in U1, whose frequency is set by C7 and R9, provides pulses to drive the gates of Q2 and Q3. The gate drive signal for Q2 is transformer coupled by T2 to isolate U1 from the high voltage present at the source and gate of Q2. The average voltage of the pulse train at the input to inductor L8 is proportional to the +18 volt output voltage from the converter. This voltage is compared to a reference voltage by an amplifier in U1, enabling U1 to establish the correct pulse width for the transistor gate drives. C6 provides a soft-start characteristic that sets the rate of voltage rise when the converter is first started.

Under conditions of very low load and high input voltages, the 18 volt output will tend to rise. Q4, CR7 and R16 comprise a shunt regulator to limit the maximum voltage to a safe value (approximately 23 volts). When load is applied, either by the battery charger of by turning on the Monitor, the voltage will return to its nominal 18 volt level.

2.4.6.3 Battery Charger

The battery charger converts +18 volts from the line power converter to a form suitable for charging the lead acid storage batteries. Output is nominally +15 volts, with current limited to 600 mA. The charger is designed to operate in both the voltage mode and current limited mode, and can efficiently provide up to 600 mA at any load voltage from 0 to 15 volts. The 18 volt input is converted to the 0 - 15 volt output required by the battery charging function by a pulse-width-modulated step-down converter. Q20, controlled by monolithic regulator IC U6, provides variable width pulses of the input voltage to L1. Filters L1 and C51 convert the pulses to a DC voltage with the same average voltage as the pulses.

When the battery is partially charged it will draw less than 600 mA from the charger. During this time the charger operates in a constant voltage mode. The output voltage is divided to 2.5 volts by R77, R78, and R79. This voltage is compared with a 2.5 volt reference voltage at U6-2. U6 adjusts the width of the pulses driving Q20 to maintain the correct output voltage. R79 is adjusted to obtain the proper regulated output voltage.

When a discharged battery is connected to the charger, it will attempt to draw a high current from the charger. This current must be limited by the charger to avoid damage to the battery or the charger. The output current of the charger flows through R75, generating a voltage proportional to the output current. This voltage is amplified by U5 and associated components and applied to the current limit input of U6. When the voltage at U6-4 reaches 200 mV, which occurs when the load current reaches 600 mA, U6 reduces the output pulse width to maintain a 200 mV maximum voltage at pin 4. The output voltage will fall to a level that will limit the current to 600 mA. As the battery charges, the voltage will rise until the voltage mode resumes control.

The battery is considered charged when it draws less than 50 mA from the charger. To avoid overcharging the battery, the battery switch board then disconnects a battery from the charger. The voltage at current sense amplifier U5-1 is proportional to the current drawn by the battery. This voltage is compared to a reference voltage by comparator op-amp U5-5,6,7. When the battery current falls below 50 mA the CHARGED signal is asserted, signalling the battery switch module to disconnect the battery.

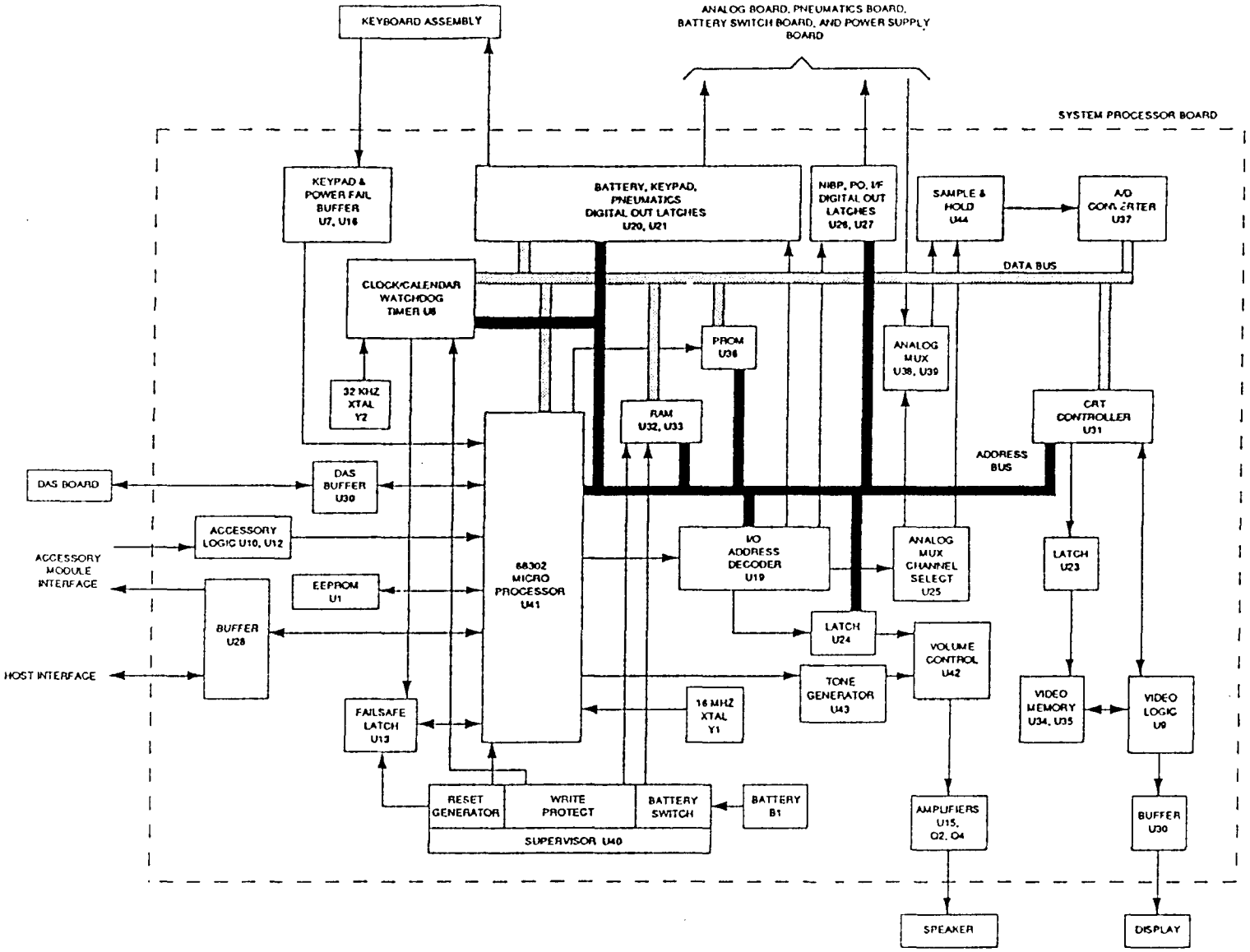
2.4.6.4 Control Logic

The control logic switches the low voltage supplies on and off in response to signals from the battery switch board, signals the CPU when power failure is impending, and signals the battery switch board when the low voltage supply has been shut-down.

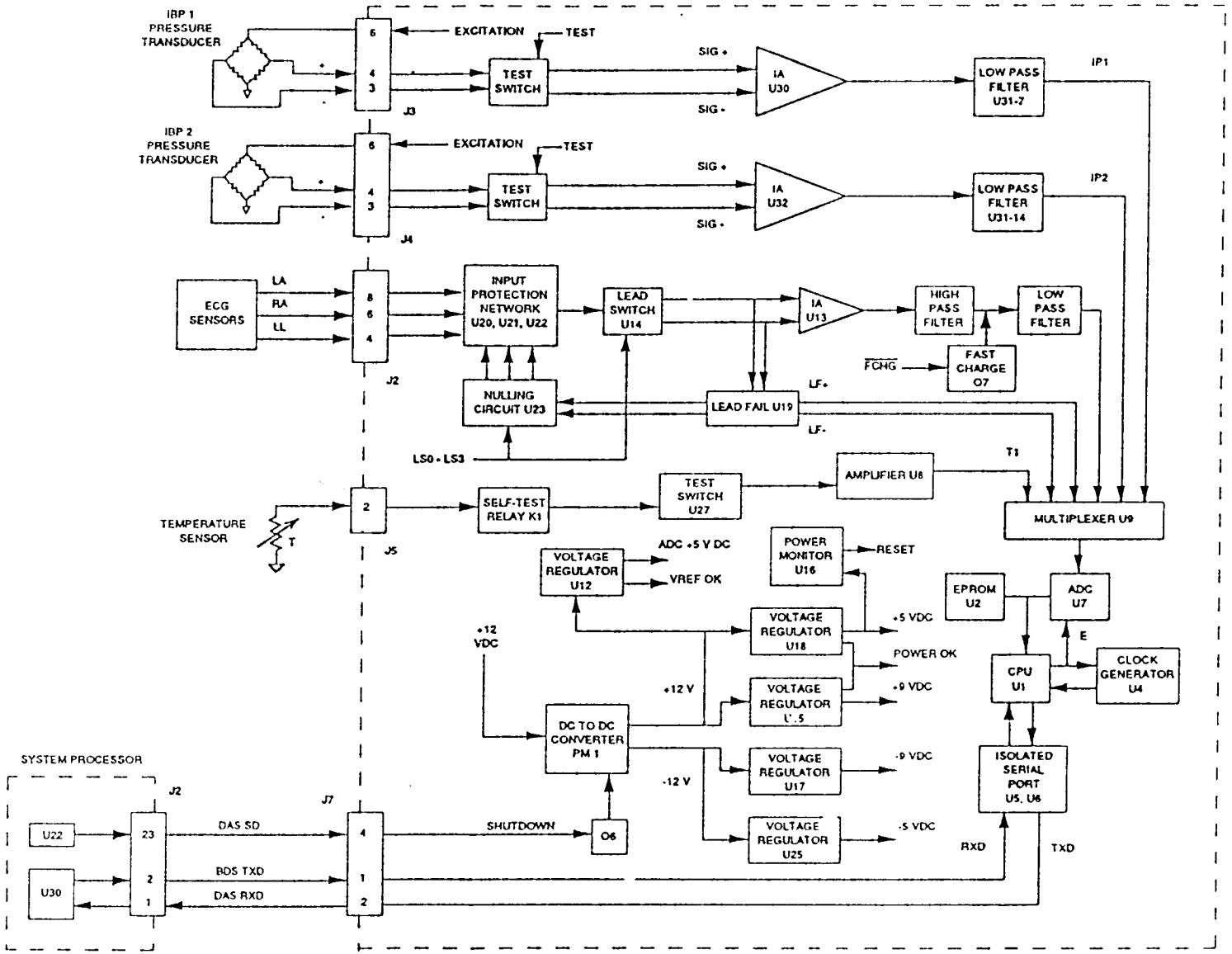
The DC input to the LV converter is compared to a reference by comparator U2-1,6,7. When the DC input falls below 9.5 volts, the comparator asserts PFI-0 (Power Fail Indicator). The CPU can suspend critical processing in anticipation of failing power, and attempt to restore power by switching to another battery if one is available. C21 stores enough energy for at least one millisecond of instrument operation, allowing time for the processor to switch batteries. The battery switch module asserts the shut-down input SD-0 when the operator presses the OFF key on the instrument panel. The resulting action is the same as previously described for low input voltage. If PFI persists for 10 to 20 milliseconds, and DC power is still available at the power supply, the output of the time delay circuit comprising comparator U2-8,9,14, R53, and C38 will go high. This will switch off the low voltage supply via shutdown input U3-16. When this occurs, Q16 turns on for 10 to 20 milliseconds and asserts OFF-0, signalling the battery switch board to lock the instrument in the OFF state until the operator again presses the ON key. This prevents the Monitor from oscillating between the ON and OFF states with a weak battery.

2.4.7 Motherboard

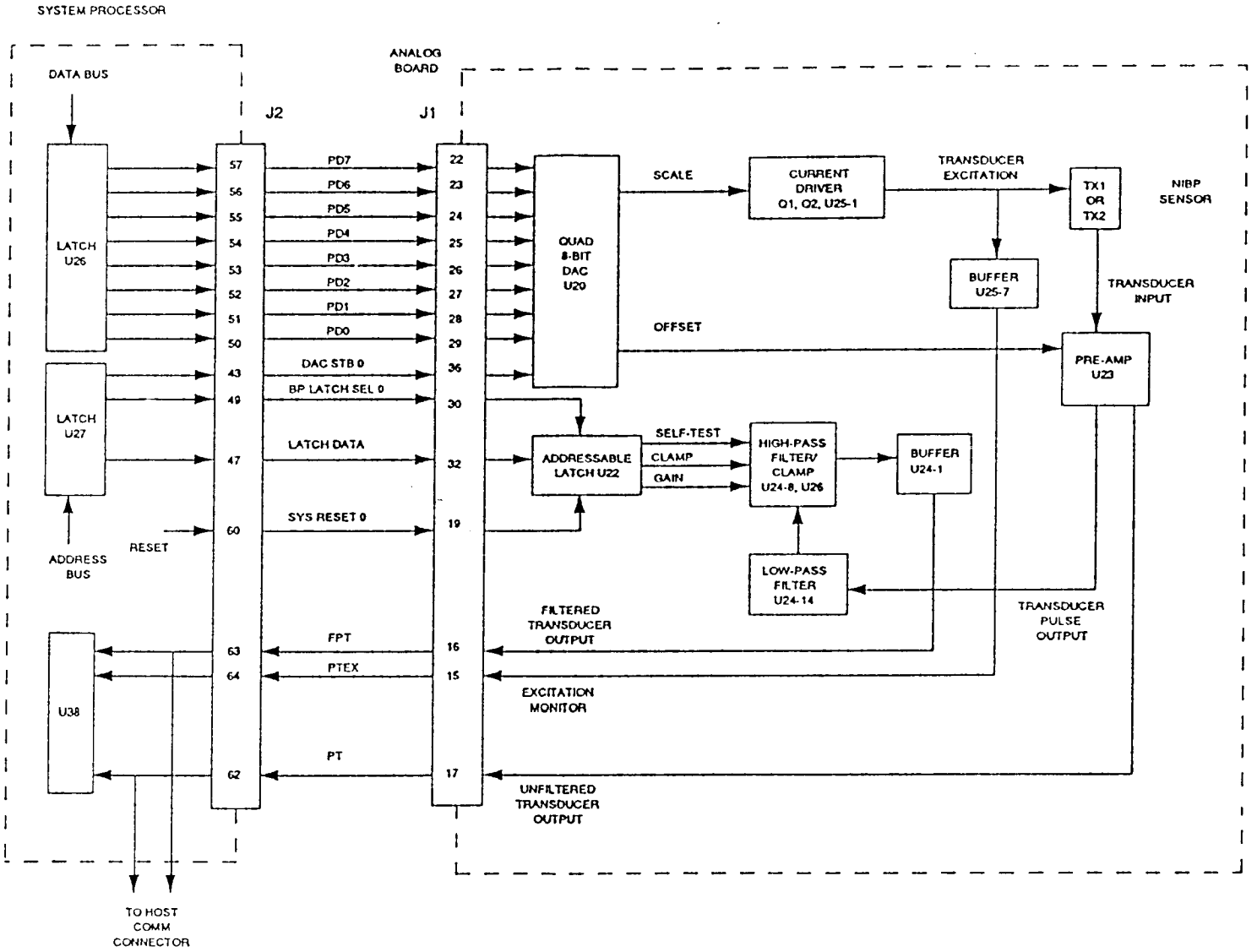
The motherboard circuits are shown on schematic SC315-373 contained in Section 4. The active components of the motherboard are limited to a fuse for each storage battery and a back-EMF diode for the fan.



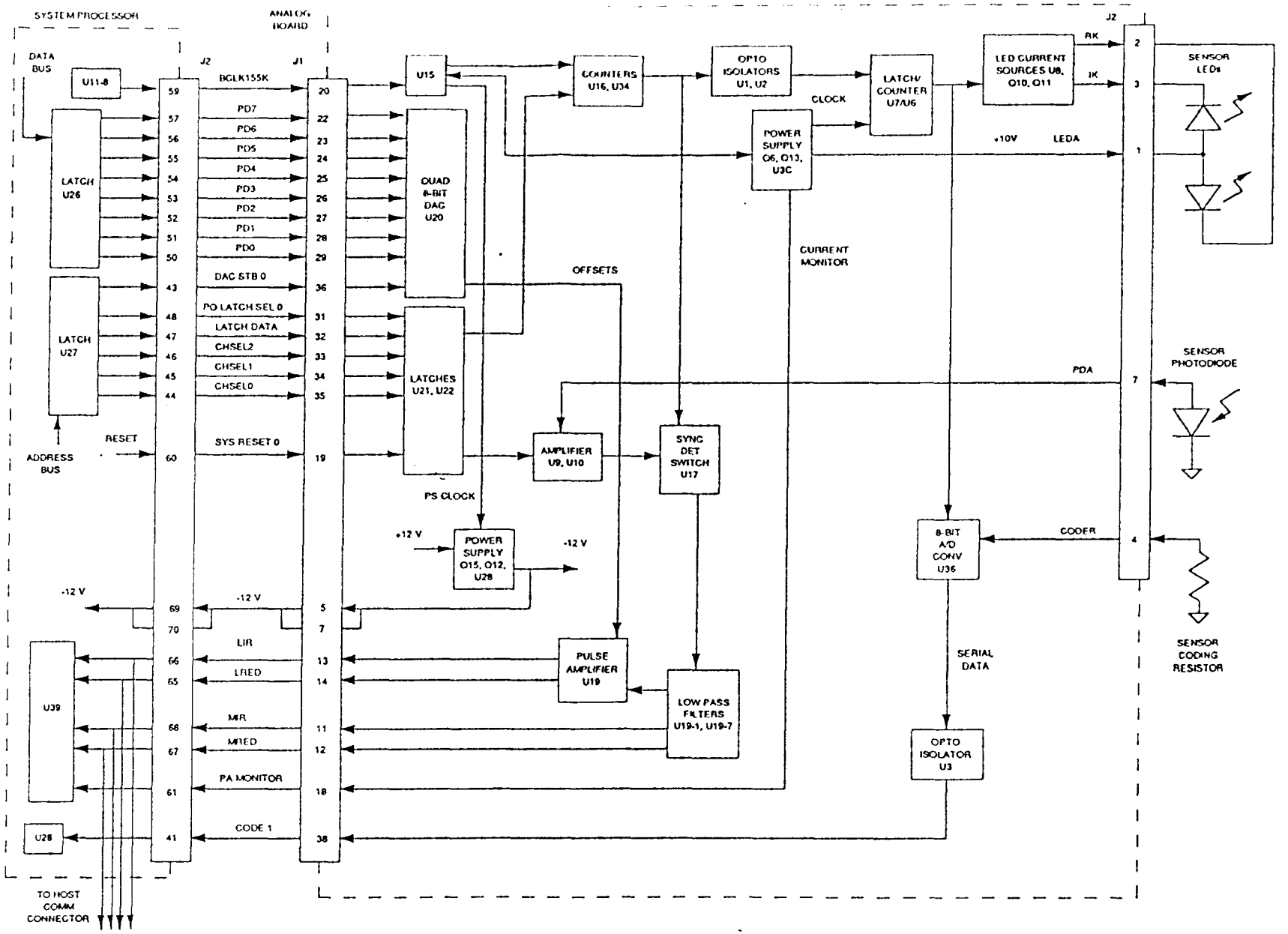
FO-1. System Processor Block Diagram



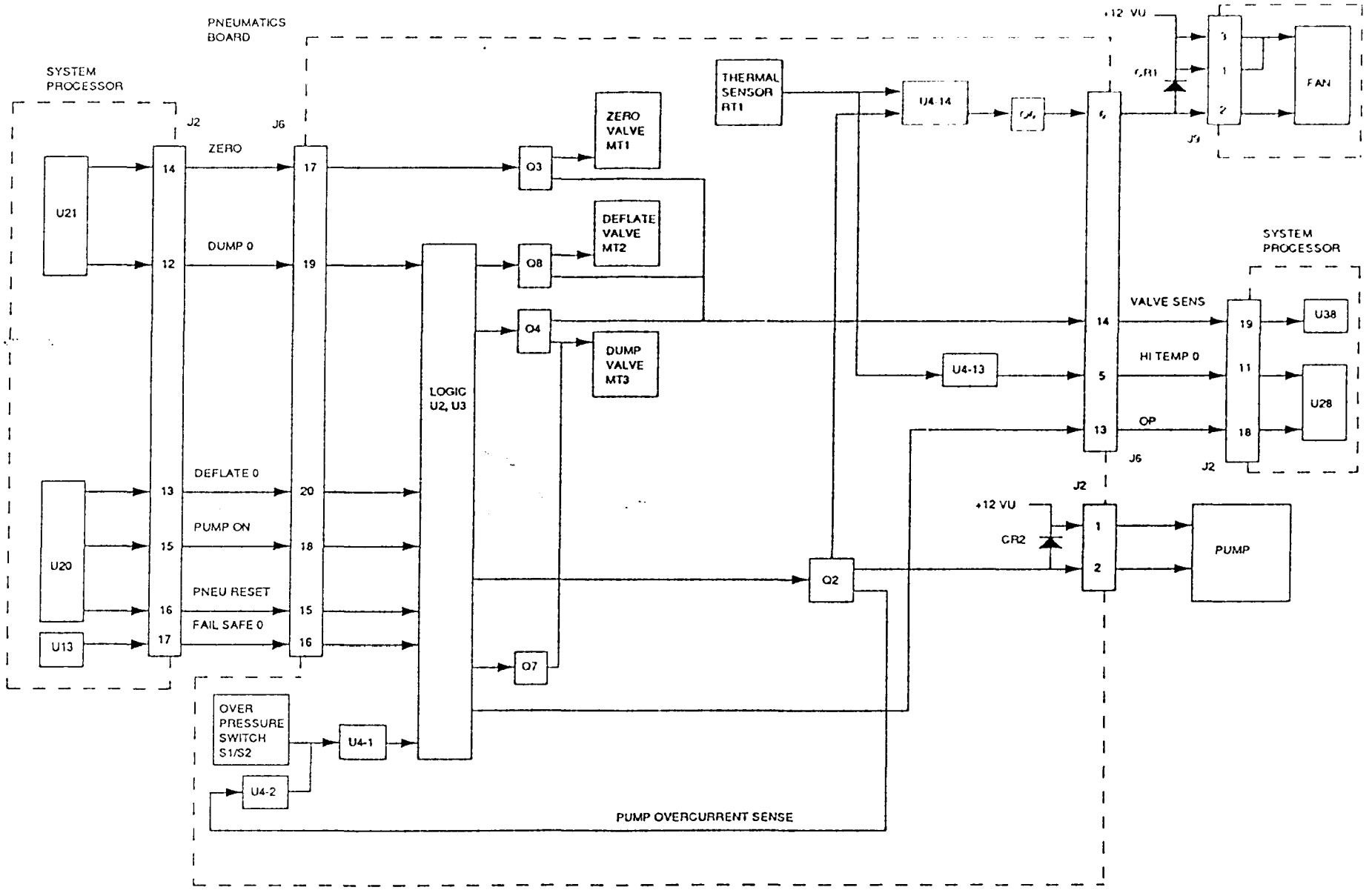
FO-2. Data Acquisition System Block Diagram



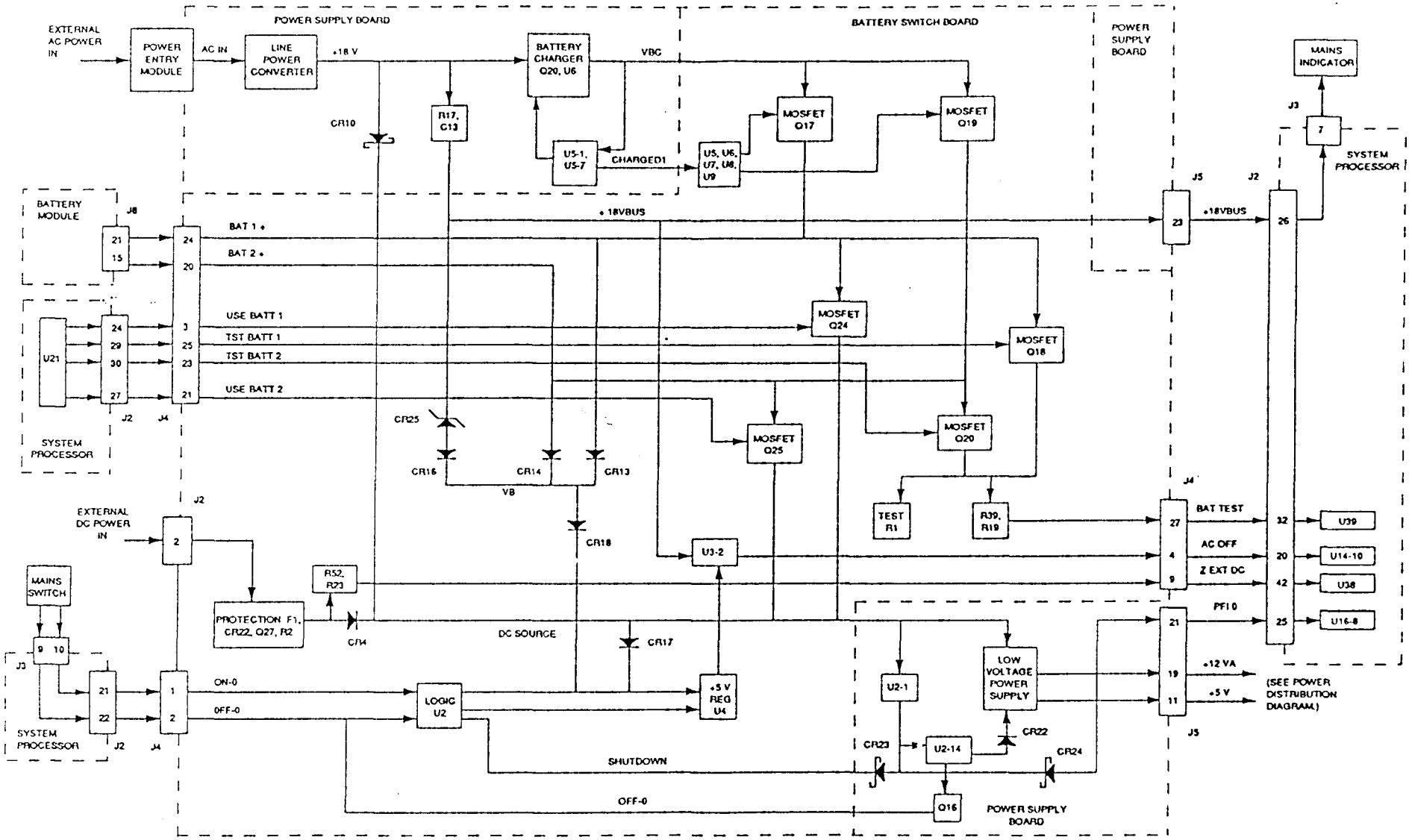
FO-4. Non-Invasive Blood Pressure System Block Diagram



FO-3. Pulse Oximetry System Block Diagram



FO-5 . Pneumatics System Block Diagram



FO-6. Power Supply Block Diagram

SECTION 3. MAINTENANCE

3.1 INTRODUCTION

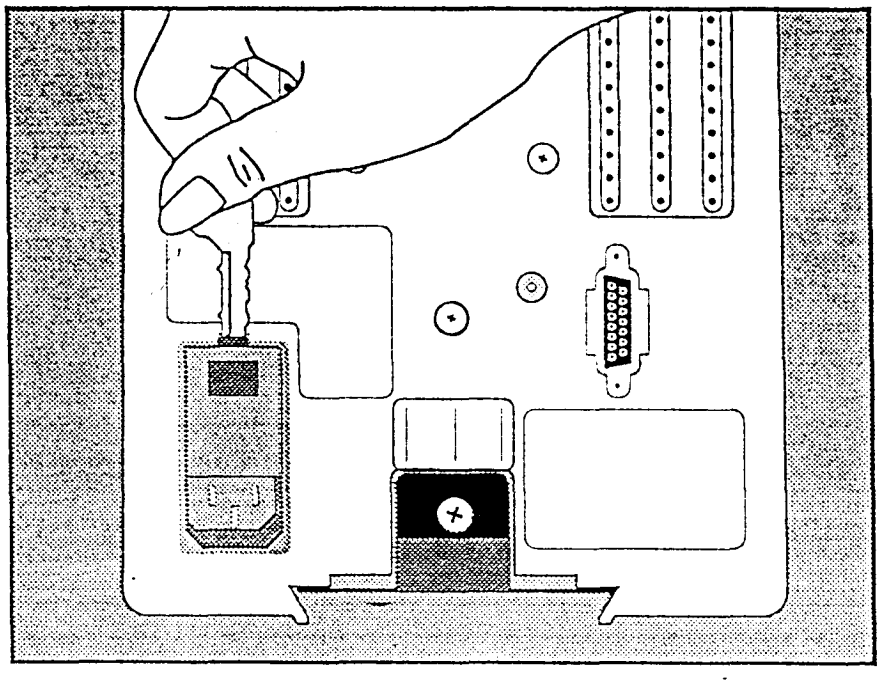
This section contains procedures for replacing fuses and backup batteries, service mode operation, periodic maintenance, calibration, and adjustment of the Monitor.

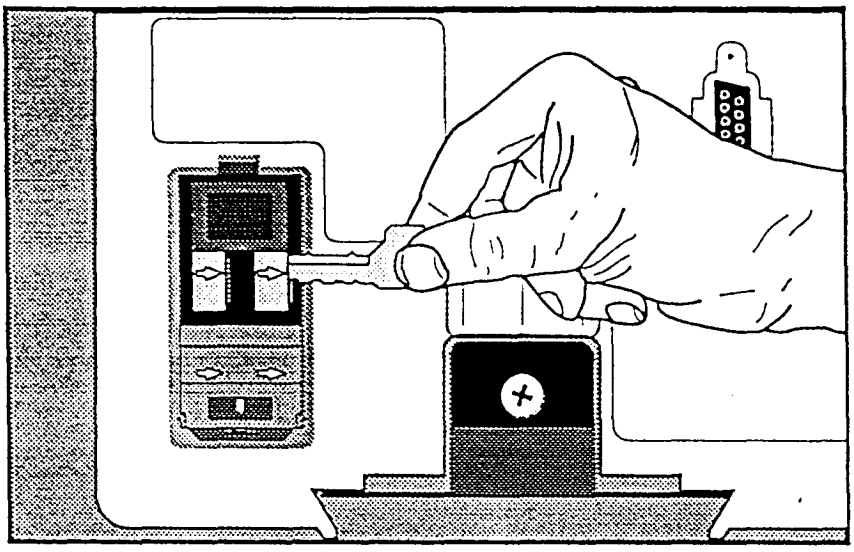
3.2 CHANGING FUSES

The Monitor contains two AC line power fuses and one fuse for each of the storage batteries.

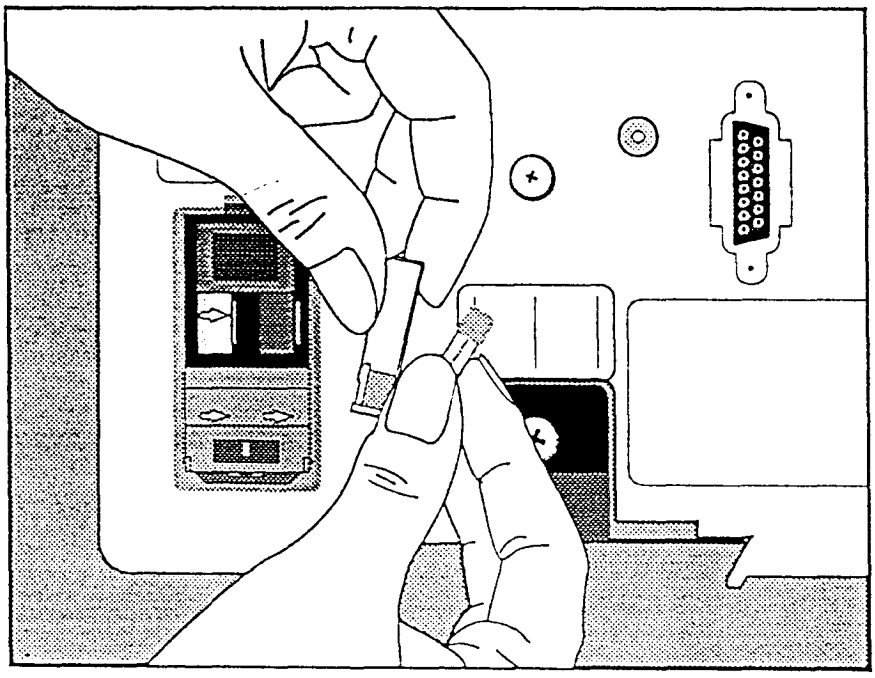
3.2.1 Line Power Fuse Replacement

If attached, unplug the power cable at the rear of the monitor. Using a flat bladed tool such as a screwdriver or a key, pry down the upper edge of the door above the power receptacle and swing the door downward on its hinge to reveal the two fuse holders.

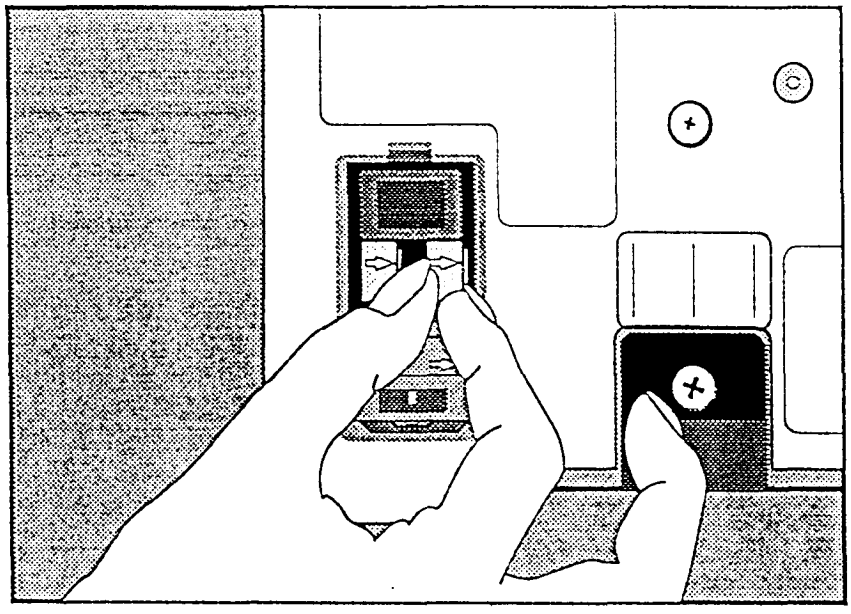




Using the same tool, apply slight sideward pressure and pry out each fuse holder.



Remove each fuse from its fuse holder and inspect it for a burned or broken filament. If the filament appears to be intact, check the fuse for continuity using an ohmmeter. Replace any blown fuses with one of the specified rating and type described on the label near the receptacle.



Reinstall each fuse and fuse holder, making sure that the arrow on the outward facing end is pointing in the same direction as the arrows on the cover plate. Snap the cover plate back into place.

3.2.2 Battery Fuse Replacement

Fuses for each of the storage batteries are mounted on the motherboard. Refer to paragraph 3.13 for disassembly procedures.

3.3 REPLACEMENT OF BACKUP BATTERY

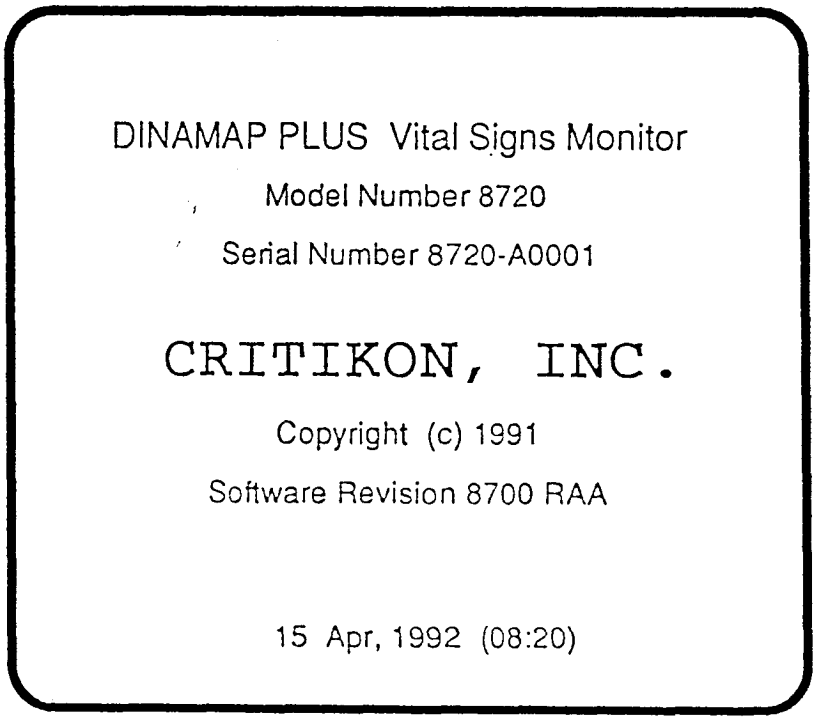
The lithium backup battery, located on the system processor board, should be replaced every two (2) years. Refer to paragraph 3.13 for disassembly procedures.

3.4 SERVICE MODE OPERATION

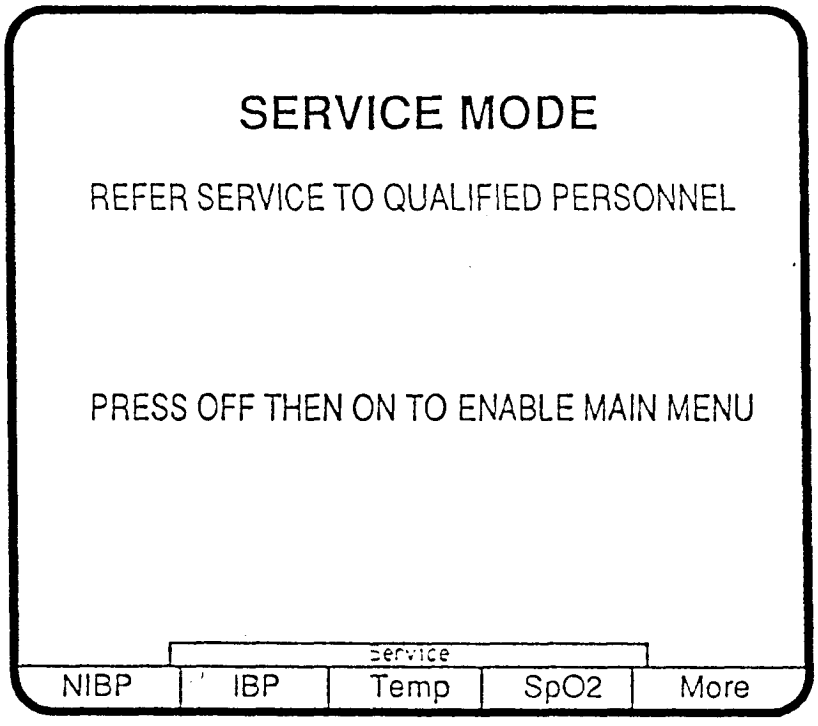
The Monitor service mode exercises the built-in diagnostic features of the unit to test key parameters. The diagnostics are intended to test both the Monitor and the patient sensors; connect as many patient sensors as possible to the unit before performing the following procedures. If any of the sensors or cuffs is not available, omit the corresponding procedure.

1. Access the service mode by turning off the Monitor, then pressing and holding the FREEZE and SILENCE keys while pressing the ON key.

2. Continue to hold the FREEZE and SILENCE keys for a few seconds while the power up screen displays and audible tones are emitted.

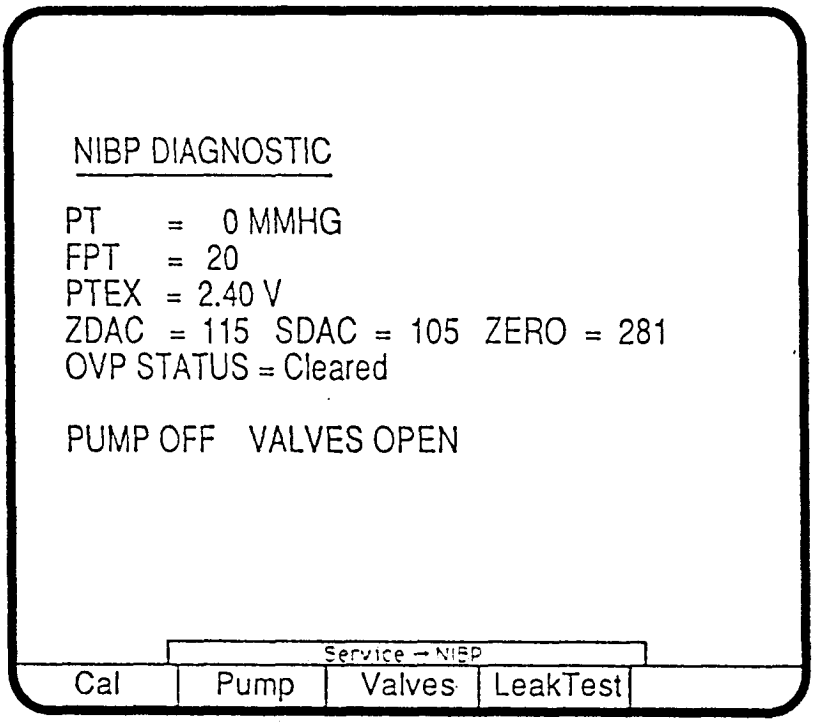


3. Release the keys after the SERVICE MODE screen shown below is displayed. While the Monitor is operating in the service mode, this screen will be displayed whenever the MAIN MENU key is pressed.



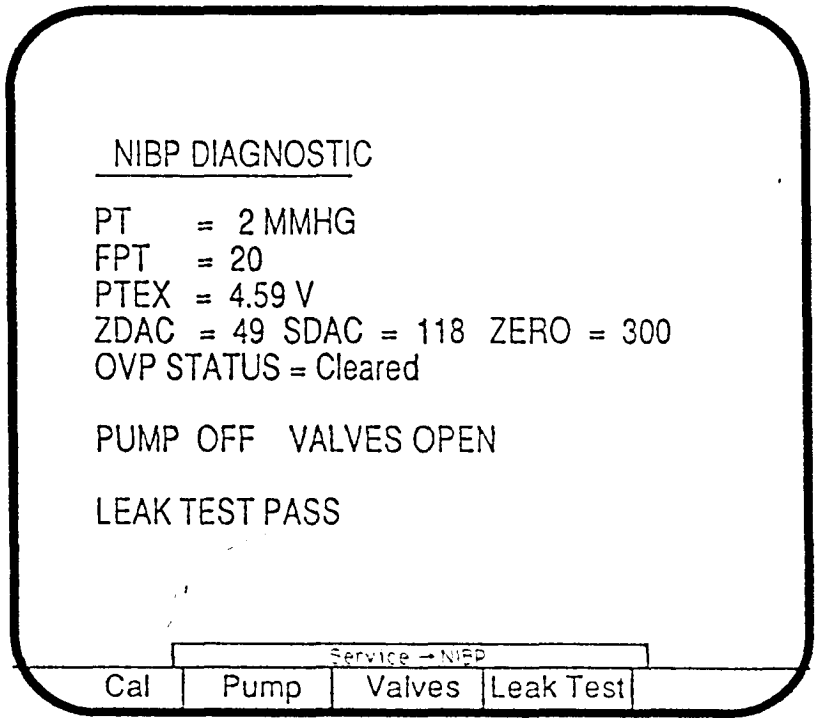
3.4.1 NIBP Tests

When the SERVICE MODE screen NIBP softkey is pressed, the following screen is initially displayed.



3.4.1.1 Automatic Leak Test

1. Press the NIBP diagnostic screen Leak Test softkey to perform an automatic leak test. While the test is underway, the message LEAK TEST IN PGRS should display. At the conclusion of the test, values similar to those shown below should be displayed.

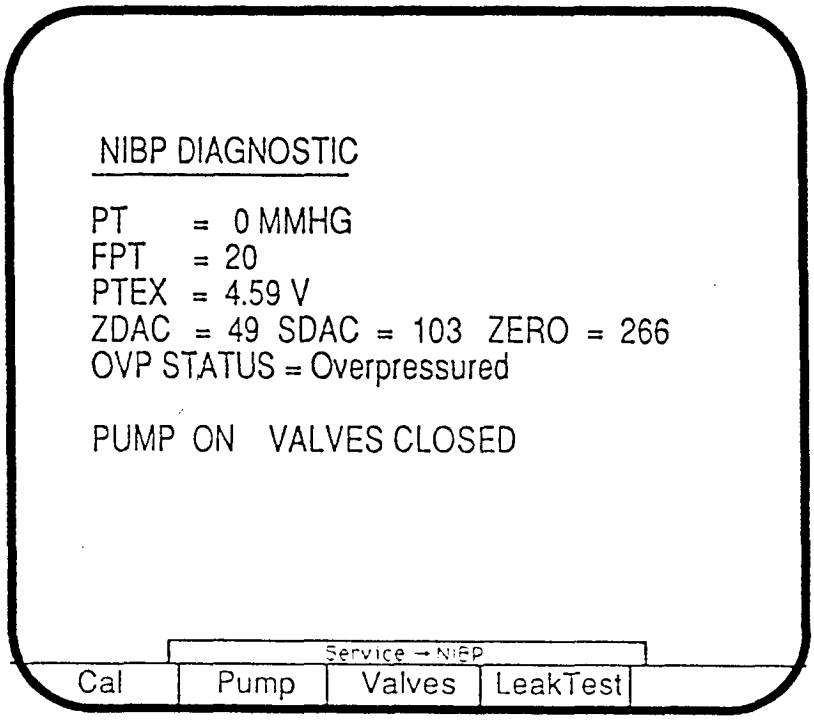


2. If the LEAK value is greater than 7 and the LEAK TEST FAIL message displays, refer to paragraph 3.6 and perform the NIBP leak test to isolate the source of the leak.

3.4.1.2 Pump Overpressure Test

This test verifies that the pump can pressure the system to the overpressure value, and that the system automatically turns off the pump.

Press the NIBP diagnostic screen Pump softkey, and observe that the pump begins to run and the value of the PT parameter displayed on the screen updates every 2 seconds. As the pressure approaches 300 mmHg, the valves should release pressure, the pump should stop, and the PT value should decrease toward zero. At the conclusion of the test, screen values similar to those shown below should be displayed.



3.4.1.3 Valves Test

1. Press the Pump key, and observe that the screen displays PUMP OFF and VALVES CLOSED.

2. Press the Valves key, and observe that PUMP OFF and VALVES OPEN are displayed.

3. Press the Pump key, and observe that PUMP ON and VALVES CLOSED are displayed, and that the pump runs.

4. Press the Pump key again, and observe that PUMP OFF and VALVES CLOSED are displayed, and the pump turns off.

5. Press the Valves key, and observe that PUMP OFF and VALVES OPEN are displayed. Observe that the valves release pressure.

3.4.1.4 Calibration Check

Check the pressure calibration of the Monitor every twelve months, or whenever there is doubt about the validity of the pressure readings.

CAUTION

Calibration equipment should always be kept dry and free of particulate matter. Moisture or foreign substances introduced into the pneumatic system can cause damage to the unit.

1. Using the calibration kit (Reorder No. 8886) supplied with the unit, an adult cuff and air hose, and a manometer, set up the equipment as shown in Figure 3-1.

2. Press the NIBP diagnostic screen Pump softkey, and observe the PT pressure indication on the screen. Press the Pump softkey when the pressure reaches approximately 250 mmHg, or let the pump shut down automatically.

3. When the pump has stopped, observe that the PT indication is within 5 mmHg of the manometer reading. If the indicated pressure is not within tolerance, perform the recalibration procedure described in paragraph 3-7.

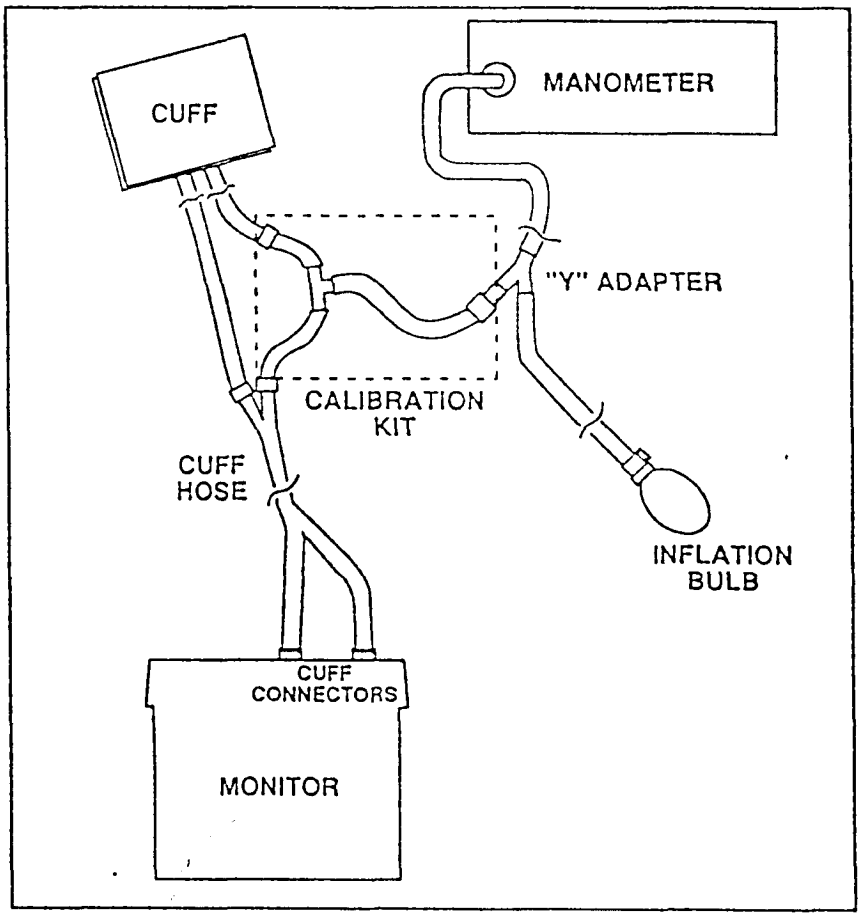


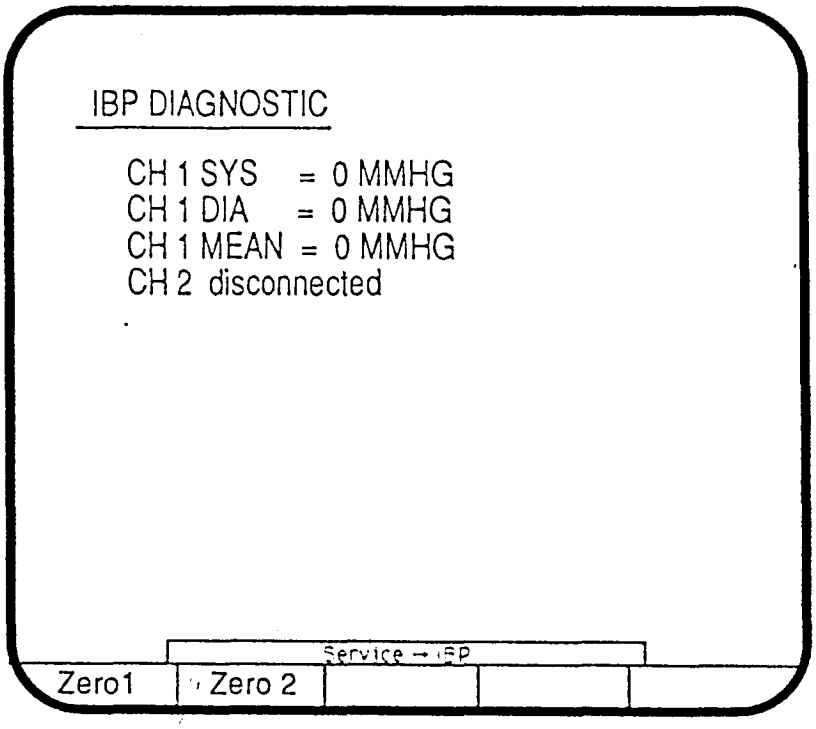
Figure 3-1. Pressure Calibration Check Setup

3.4.2 IBP Tests

The IBP tests (Model 8720) set the zero reference for the IBP channels.

1. Press the SERVICE MODE screen IBP softkey, and observe that the following screen is displayed. Initially, each channel parameter should indicate --- MMHG.

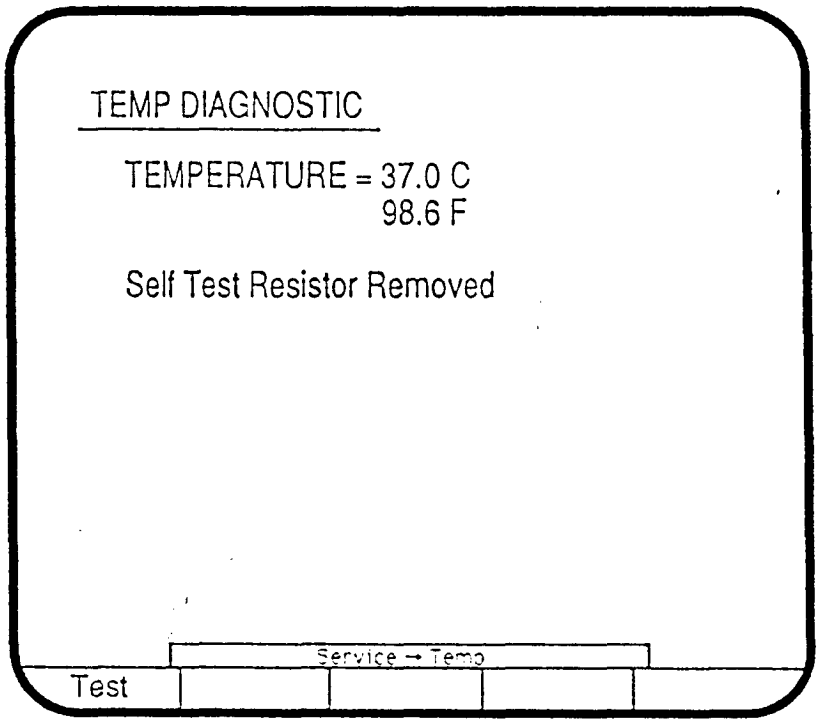
2. Press the corresponding Zero softkey, and observe that the zero values shown below are displayed. If the sensor is connected to the other channel input and the other softkey is pressed, the indications shown above should display for the other channel.



3.4.3 Temperature Tests

The temperature test (Model 8720) verifies the accuracy of the temperature channel.

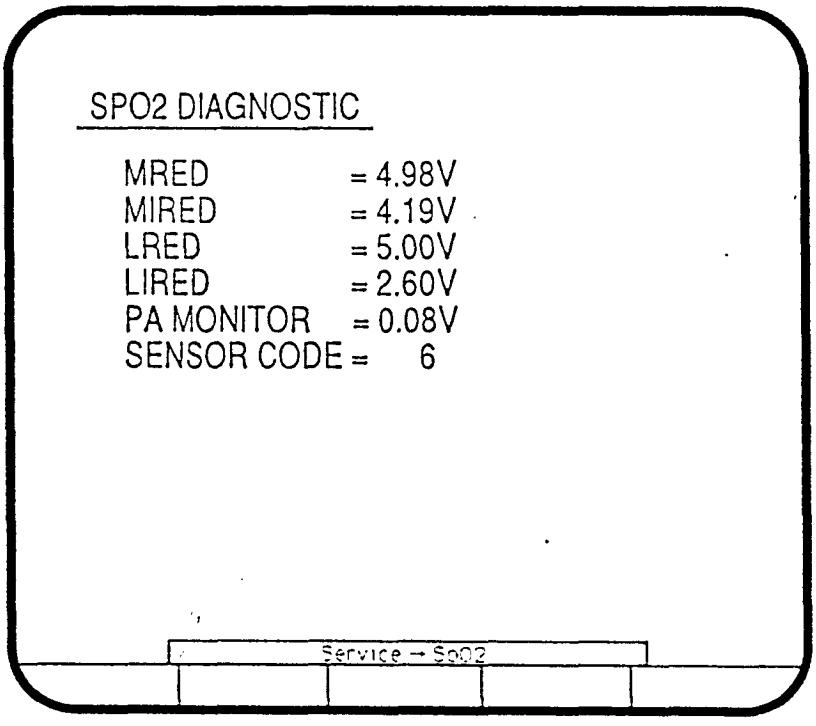
1. Press the SERVICE MODE screen Temp softkey, and observe that the following screen is initially displayed if a temperature probe is connected (if not connected, INACTIVE is displayed).



2. Press the Test softkey, and observe that the screen changes to display the Self Test Res. In Place - Expect 37.1C message. Observe that the probe temperature is within ±0.2 C of 37.1 C.

3.4.4 SpO2 Test

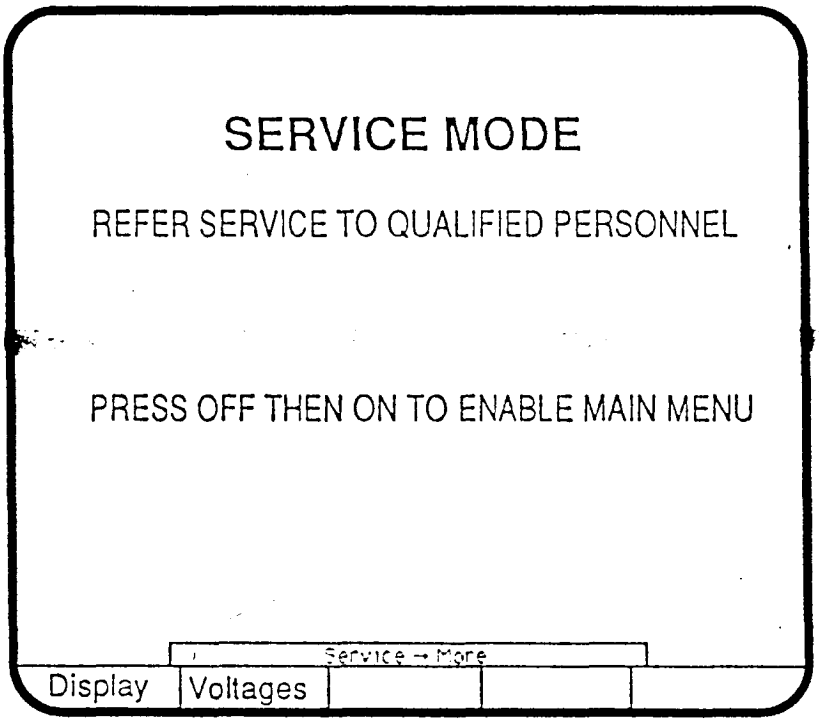
Check the pulse oximetry channel by pressing the SERVICE MODE screen SpO2 softkey and observing that the following screen appears. Initially, 0V should be displayed for each parameter, then (if a sensor is connected) values similar to those shown below should display. The SENSOR CODE initially should display Sensor Unplugged before indicating a sensor code number such as 6 (varies with sensor type).



3.4.5 More Tests

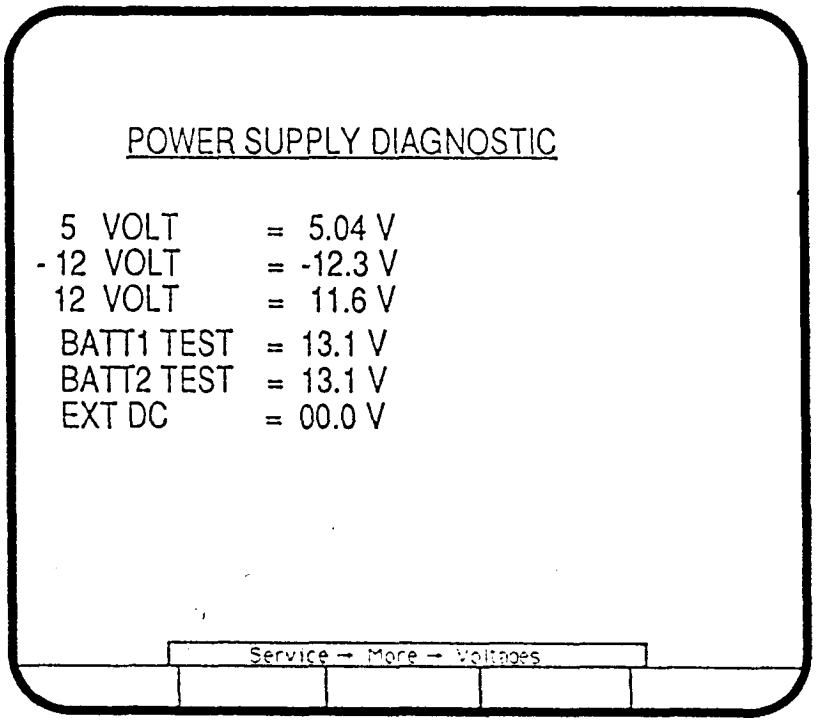
These tests verify operation of the display screen segments and power supply.

1. Press the SERVICE MODE screen More softkey, and observe that the following screen is initially displayed.



2. Press the More screen Display softkey, and observe that the Monitor runs checkerboard test patterns, to help determine whether any screen segments are not being displayed.

3. Press the PRIOR MENU key to return to the More screen. Press the Voltage softkey, and observe that values similar to those shown below appear. If the Monitor is connected to an external DC source, the external source voltage should be displayed. If any storage batteries are removed, the corresponding battery voltage should show -- V.


POWER SUPPLY DIAGNOSTIC
5 VOLT = 5.04 V
-12 VOLT = -12.3 V
12 VOLT = 11.6 V
BATT1 TEST = 13.1 V
BATT2 TEST = 13.1 V
EXT DC = 00.0 V
Service → More → Voltages

3.4.6 Service Mode Exit

To exit the service mode, recycle the Monitor OFF and ON power keys.

3.5 PERIODIC MAINTENANCE

3.5.1 As Required

Perform the following maintenance procedures whenever required.

3.5.1.1 Integrity of Hoses and Cuffs

When there is doubt about the pneumatic integrity of any NIBP cuff and hose, perform the NIBP leak test, paragraph 3.6.

3.5.1.2 Cleaning of Monitor

Wipe the exterior of the Monitor with a cloth slightly dampened with mild detergent or normal hospital bacteriocides. Use dishwashing detergents such as IVORY and JOY (registered trademarks of Proctor and Gamble Corp.), or PALMOLIVE (registered trademark of Colgate-Palmolive Corp.)

Do not immerse unit.

Do not clean unit with isopropyl alcohol or other solvents.

3.5.1.3 Cleaning of Accessories

Clean the adult cuffs supplied for use with the monitor by hand washing in warm, soapy water. However, take care to avoid entry of water into the cuff and hoses at any time. If water enters the cuff, dry the cuff by passing air through it.

The neonatal cuffs are for single patient use - discard if they become soiled.

Clean cuffs and hoses with a cloth slightly dampened with mild detergent

Do not immerse hoses.

Do not immerse cuffs without prior application of cuff hose caps.

Clean SpO2 sensor surface before and after each patient use. Clean SpO2 sensor with a cloth slightly dampened with a mild detergent. Wipe SpO2 sensor to ensure all detergent residue has been removed.

Follow manufacturer's instructions for cleaning ECG lead wires and cable.

Compatible cleaning and disinfecting solutions are:

Dishwashing detergents such as IVORY and JOY (registered trademarks of Proctor and Gamble Corp.), or PALMOLIVE (registered trademark of Colgate-Palmolive Corp.)

Chlorine bleach disinfectant, 5.25%, various brands, 0.75 cup per gallon of water

Isopropyl alcohol

Cidex Formula 7 (registered trademark of Surgikos, Inc.) or pHisoHex (registered trademark of Winthrop-Breon Laboratories)

Quatenary-based germicidal detergents like VESTAL INSURANCE (registered trademark of the Vestal Corp.), HI-TOR PLUS (registered trademark of the Huntington Corp.), or VIREX (registered trademark of S.C. Johnson & Son Corp.)

For the above, follow manufacturers' recommendations for dilution rate and use. These recommendations are not an endorsement of the manufacturers or of the effectiveness of these materials for cleaning or disinfecting.

3.5.1.4 Storage of Monitor

If it becomes necessary to store the Monitor for an extended period of time, disconnect optional modules and remove batteries from modules. Replace the cover access plate, attach the original packing inserts, and place the unit into the original shipping carton.

3.5.2 Annual Procedures

Perform the NIBP calibration test procedure (paragraph 3.4.1.4) every twelve months, or whenever the accuracy of the NIBP readings is in doubt. If required, perform the recalibration procedure described in paragraph 3.7.

3.6 NIBP LEAK TEST

Check the cuff and hose for air leaks whenever there is doubt about their pneumatic integrity. Proceed as follows:

CAUTION

Calibration equipment should always be kept dry and free of particulate matter. Moisture or foreign substances introduced into the pneumatic system can cause damage to the unit.

1. Using the calibration kit (Reorder No. 8886) supplied with the unit, an adult cuff and air hose, and a manometer, set up the equipment as shown in Figure 3-2.

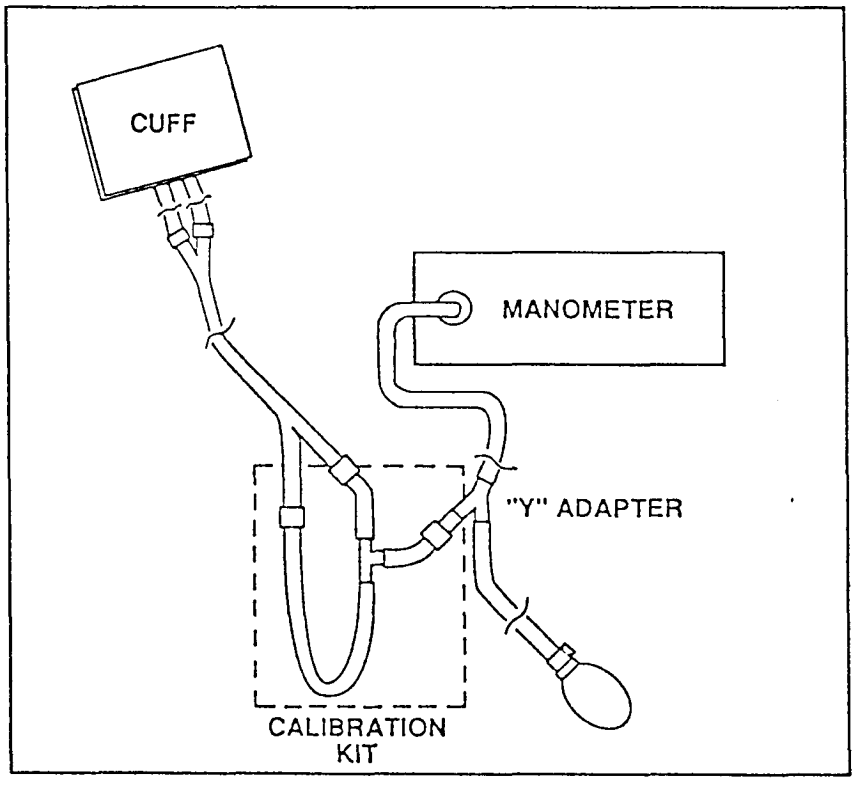


Figure 3-2. Cuff and Hose Leak Test Setup

2. Close the pressure release valve on the manometer inflation bulb and slowly pump up the pressure until the manometer indicates 200 mmHg ±1 mmHg.

3. Verify that the pressure indicated on the manometer remains within 5 mmHg of 200 mmHg for 60 seconds. If not, either the cuff or hose or both are defective. If the cuff and hose pass this test, reconnect the setup shown in Figure 3-1. Pump up the cuff and hose to 200 mmHg ±1 mmHg and repeat the leak test to try to isolate the leak to the Monitor. Repeat the leak check for all cuff and hose combinations used with the Monitor.

3.7 NIBP RECALIBRATION

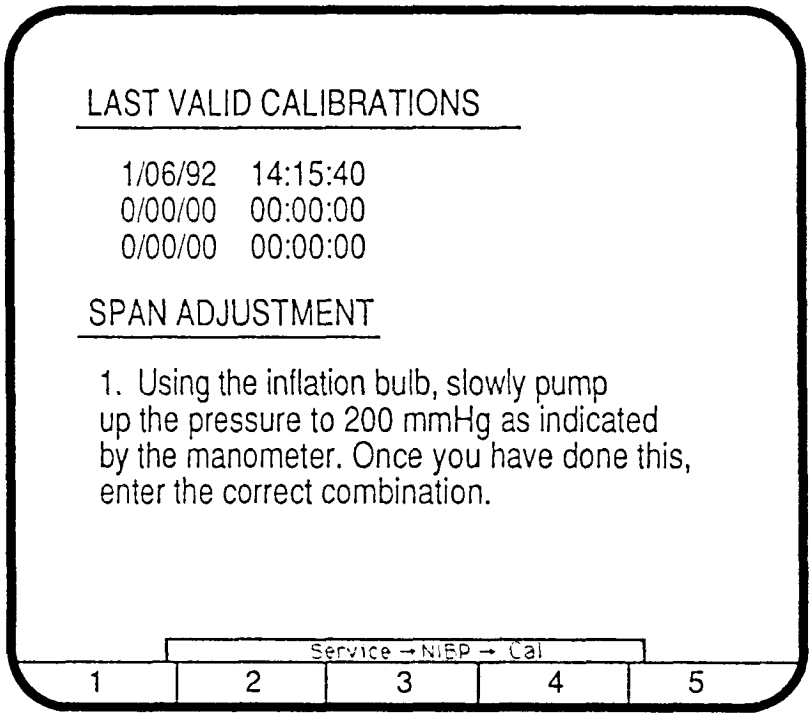
Using the procedure described in paragraph 3.4.1.4, check pressure calibration of the Monitor every twelve months, or whenever there is doubt about the validity of the pressure readings. If the indicated pressure is not within tolerance, recalibrate the Monitor as follows:

CAUTION

Calibration equipment should always be kept dry and free of particulate matter. Moisture or foreign substances introduced into the pneumatic system can cause damage to the unit.

1. Using the calibration kit (Reorder No. 8886) supplied with the unit, an adult cuff and air hose, and a manometer, set up the equipment as shown in Figure 3-1.

2. Press the NIBP diagnostic screen Cal softkey, and observe that the following screen is displayed.


LAST VALID CALIBRATIONS
1/06/92 14:15:40
0/00/00 00:00:00
0/00/00 00:00:00
SPAN ADJUSTMENT
1. Using the inflation bulb, slowly pump up the pressure to 200 mmHg as indicated by the manometer. Once you have done this, enter the correct combination.
Service → NIBP → Cal
1
2
3
4
5

3. Fold the adult cuff so the index line is aligned with the inner range mark on the inside of the cuff.

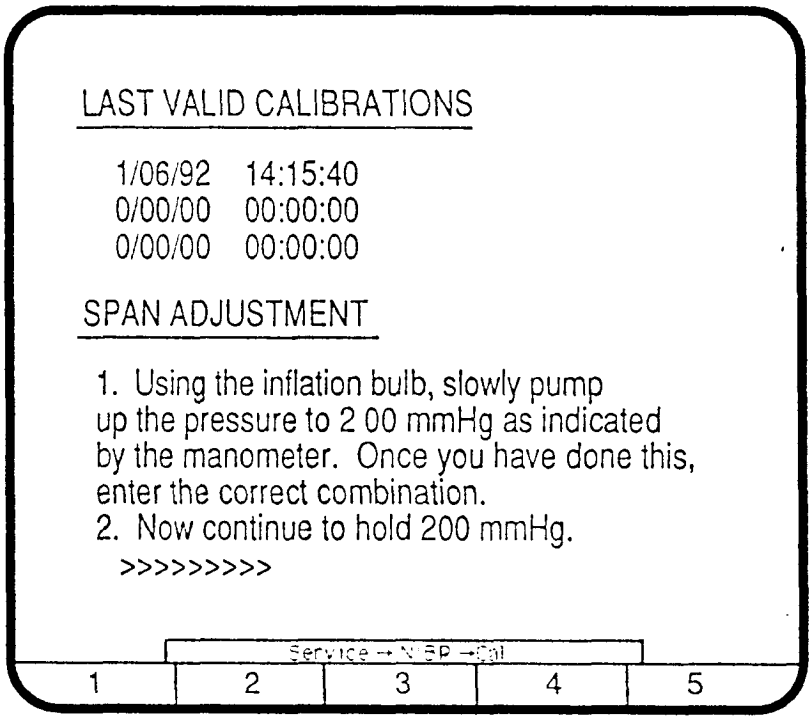
4. Close pneumatic release valve on manometer bulb. Using the inflation bulb, manually pump up the pressure until the manometer indicates 200 mmHg ±1 mmHg.

5. While continuing with the following procedure, observe whether the pressure indicated on the manometer remains within 5 mmHg of 200 mmHg for 60 seconds.

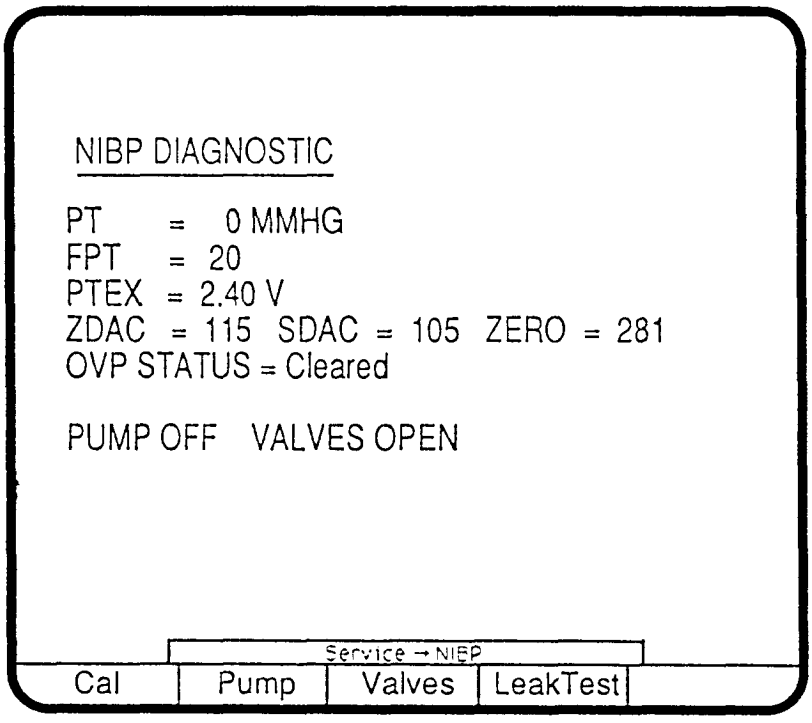
NOTE

If the leakdown is greater than 5 mmHg in 60 seconds, isolate the source of the leak to either the cuff and hose or the Monitor by performing the leak test procedure described in Paragraph 3-6.

6. Using the five numbered softkeys, enter the number 4113 and observe that the following screen is displayed. The advancing line of arrows displayed near the bottom of the screen indicate that the calibration is being calculated.


LAST VALID CALIBRATIONS
1/06/92 14:15:40
0/00/00 00:00:00
0/00/00 00:00:00
SPAN ADJUSTMENT
1. Using the inflation bulb, slowly pump up the pressure to 2 00 mmHg as indicated by the manometer. Once you have done this, enter the correct combination.
2. Now continue to hold 200 mmHg.
>>>>>>>>>
1
2
3
4
5

7. Observe that the following screen is displayed after the calibration calculation is completed.



8. Disconnect the test setup, and reconnect the cuff and hose to the Monitor.

3.8 ALIGNMENT AND ADJUSTMENT

Ensure that a digital voltmeter (Fluke 8020 or equivalent) is available before attempting any alignment or adjustment procedures. Refer to paragraph 3.13 for disassembly procedures.

3.8.1 Five Volt Logic Power Supply

The +5 VDC logic supply is adjusted by R46 on the power supply board. Refer to paragraph 3.13 for disassembly procedures. Refer to Section 4 for illustration.

Although the +5 VDC supply depends on the +12 VDC supply for source voltage, it is not necessary to recheck the accuracy of the +12 VDC supply (paragraph 3.8.3) at this time unless a gross readjustment of the +12 VDC supply was required.

Perform the following procedure:

1. Connect the voltmeter positive lead to TP2.
2. Connect the negative lead to chassis ground.
3. Ensure that a charged storage battery is installed, or that the Monitor is connected to an external ac or dc power source.
4. Apply power by pressing the ON key on the control panel.
5. Observe that the voltmeter indicates +5.0 Vdc ±0.05 Vdc. If necessary, adjust R46 to obtain this reading.

3.8.2 Battery Charger Float Voltage

The battery charger voltage is adjusted by R79 on the power supply board. Refer to paragraph 3.13 for disassembly procedures. Refer to Section 4 for illustration.

Perform the following procedure:

1. Remove storage batteries from the battery module, if any. Disconnect any other accessory modules.
2. Disconnect the Monitor from any external source of power.

3. Connect a 75-ohm (±10%), 5-Watt load resistor between TP4 and TP1 on the power supply board.

4. Connect the voltmeter positive lead to TP4.

5. Connect the negative lead to TP1.

6. Connect the Monitor to an external ac power source of 95 to 255 VAC, 47 to 63 Hz.

7. Observe that the voltmeter indicates +15.0 Vdc ±0.05 Vdc. If necessary, adjust R79 to obtain this reading.

3.8.3 Twelve Volt Analog Power Supply

The +12 VDC logic supply is adjusted by R22 on the power supply board. Refer to paragraph 3.13 for disassembly procedures. Refer to Section 4 for illustration.

Since the +5 VDC supply depends on the +12 VDC supply for source voltage, the accuracy of the +5 VDC supply adjustment (paragraph 3.8.1) should be rechecked if the +12 VDC supply has been repaired or if gross readjustment of the +12 VDC supply is required.

Perform the following procedure:

1. Connect the voltmeter positive lead to TP3.

2. Connect the negative lead to chassis ground.

3. Ensure that a charged storage battery is installed, or that the Monitor is connected to an external ac or dc power source.

4. Apply power by pressing the ON key on the control panel.

5. Observe that the voltmeter indicates +12.0 Vdc ±0.05 Vdc. If necessary, adjust R22 to obtain this reading.

3.8.4 Pneumatics System Pressure Switch

During the initial warranty period, the recommended procedure for repair of a defective pneumatics board overpressure switch is limited to replacement of the pneumatics board. At the time of publication, procedures for adjustment or replacement of the overpressure switch were under review.

3.8.5 Pulse Oximeter Tuned Transformers

During the initial warranty period, the recommended procedure for repair of defective analog board tuned transformers T1 and T2 is limited to replacement of the analog board. At the time of publication, procedures for adjustment of the tuned transformers were under review.

3.9 JUMPER OPTIONS

Information about the jumper reconfigurations required for alternate NIBP sensors is shown on schematic SC315-334 contained in Section 4.

3.10 ALARM CODE INTERPRETATION

System hardware alarm codes are listed in Table 3-1. Refer to the Operation Manual for information about patient alarms and procedural alarms. DAS alarms do not apply to the model 8700 Monitor. IBP and temperature alarms apply only to the model 8720 Monitor.

Table 3-1. System Error Alarms

CODE	NAME	DESCRIPTION
D-10	DAS ROM checksum	Failure of DAS EPROM power up checksum test
D-12	DAS A/D calibration	Failure to complete DAS A/D converter power up self calibration
D-21	DAS +5 or +9 VDC	Failure of DAS positive 5 VDC or 9 VDC power supplies
D-22	DAS -5 or -9 VDC	Failure of DAS negative 5 VDC or 9 VDC power supplies
D-66	DAS RAM test	Failure of DAS processor internal RAM power up test
I-31	IBP1 gain	Failure of IBP channel one gain test at power up or when sensor connected
I-32	IBP2 gain	Failure of IBP channel two gain test at power up or when sensor connected
I-41	IBP1 offset	Failure of IBP channel one offset test at power up or when sensor connected
I-42	IBP2 offset	Failure of IBP channel two offset test at power up or when sensor connected
I-51	IBP1 frequency	Failure of IBP channel one step response test at power up or when sensor connected
I-52	IBP2 frequency	Failure of IBP channel two step response test at power up or when sensor connected

Table 3-1. System Error Alarms (Continued)

CODE	NAME	DESCRIPTION
N-12	NIBP PT excitation	Failure of NIBP pressure transducer SDAC PTEX check, tested prior to each determination and every 5 minutes
N-26	NIBP autozero	Failure of PT test with auto zero valve open (autozero valve may be defective), tested after each determination
N-41	NIBP PT offset	Failure of PT offset test with zero valve open, tested after PT excitation test prior to each determination and every 5 minutes
N-51	NIBP FPT pulse test	Failure of filtered PT channel pulse test, tested at power up and autozero check following each non-stat determination
P-11	SpO2 LED current sense	Excessive current drain at LED drive and power supply circuit
P-22	SpO2 M channel zero	Failure of M channel offset, tested with LED off and minimum gain
P-31	SpO2 LIR gain	Excessive gain at infrared L channel amplifier
P-32	SpO2 LRED gain	Excessive gain at red L channel amplifier

Table 3-1. System Error Alarms (Continued)

CODE	NAME	DESCRIPTION
P-33	SpO2 red M to L gain	Failure of test comparing gain of red M channel and L channel
P-34	SpO2 infrared M to L gain	Failure of test comparing gain of infrared M channel and L channel
P-51	SpO2 L to IR frequency	Failure of infrared L channel filter pulse test
P-52	SpO2 L to RED frequency	Failure of red L channel filter pulse test
S-02	System DAS clock	DAS data block rate out of 394 to 406 per second range
S-11	System power supply	Failure of one of +5 VDC, +12 VDC, or -12 VDC system power supplies
S-22	System overtemperature	Sensor on pneumatics board detects temperature than 70° C, or board is not installed
S-66	System RAM test	Failure of system RAM power up test
S-77	System ROM checksum	Failure of system ROM checksum, tested at power up and in background
S-92	System DAS serial comm	Failure of DAS to respond within one second to restart command
T-21	Temperature reference	Failure of temperature reference resistor substitution check, tested at power up and on demand via service mode
T-41	Temperature offset	Failure of temperature circuit power up offset test

3.11 CARE OF STORAGE BATTERIES

The storage battery specified for use with the DINAMAP™ *PLUS* Monitor is a sealed lead-acid battery.

NOTE

To obtain maximum battery life, the battery should be fully charged as soon as possible after each use.

The expected battery cycle life is largely dependent on the way the battery is used. If the battery is allowed to be fully discharged after each use and then fully recharged soon after use, the battery should last for the full two hundred recharge life cycle. If a battery is used in the top one third of its charge and fully charged whenever possible, up to twelve hundred cycles can be expected, approximately six times the number of cycles used to 100% capacity.

If any storage batteries are in the battery module while the Monitor is connected to an external AC power source (even if the Monitor is off) the monitor will attempt to charge the batteries.

While the charger is idle, the charge control circuit checks every five minutes to see if there are any uncharged batteries in the module. Therefore, it may take up to five minutes for battery recharging to begin after the batteries are removed and replaced.

Since the charger automatically disconnects from each battery when the battery is fully charged, batteries left in the module should not be adversely affected.

A battery that has been fully discharged can be fully charged by the Monitor in less than five hours. If more than one battery is to be charged, the Monitor will automatically charge the second battery after the first battery either becomes fully charged or is removed from the battery module.

A fully charged battery can be stored up to six months and retain as much as 80% of its capacity.

NOTE

Storage of batteries at temperatures above 25°C can dramatically increase the rate of self discharge for the battery.

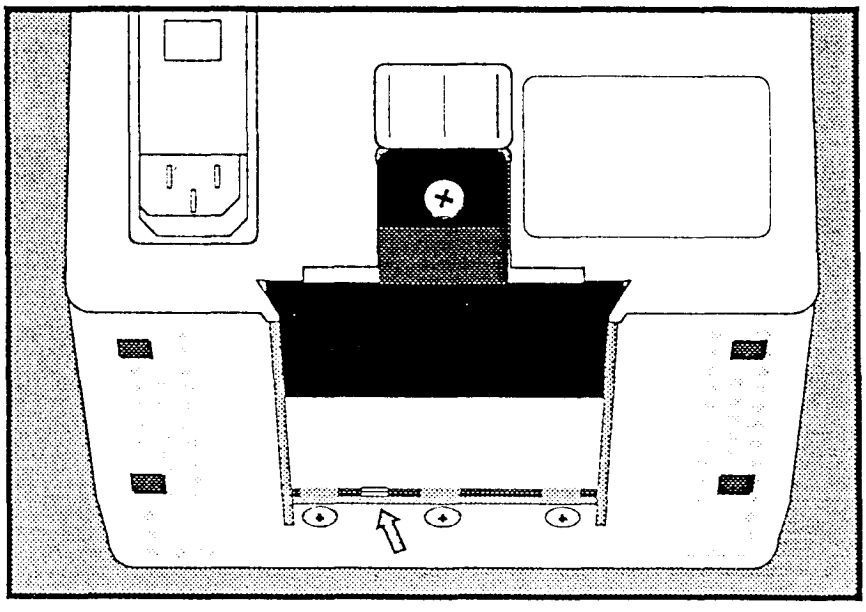
Take care not to leave a battery in the discharged state for any extended period of time, or the normal cycle life of the battery may be drastically reduced.

One fully charged battery will supply enough energy to operate the Monitor for approximately one hour. This operation would include continuous ECG, invasive blood pressure, temperature, pulse oximetery and non-invasive blood pressure operations set at five minute determinations.

3.12 GROUND RESISTANCE TEST

Using a safety analyzer (Dynatech Nevada Model 432HD or equivalent), proceed as follows to check the ground resistance of the Monitor:

1. On the safety analyzer, set the MODE switch to Power Cord Resistance.
2. Turn off the safety analyzer test receptacle.
3. Connect Monitor under test AC power cord to safety analyzer.
4. Connect safety analyzer Kelvin cable between the red Current Meter jack and the ground clip (indicated by arrow in figure below) on the underside of the Monitor under test. Use a screwdriver or other tool as a probe to make contact with the ground clip.
5. Turn on the safety analyzer, and note that the indicated resistance is less than 0.1 ohm.



3.13 DISASSEMBLY PROCEDURES

1. Remove the 1/4-20 x 5/8" screw (Figure 4-1) that attaches the access plate (or accessory module). Remove the plate or module.
2. Remove the two fasteners that attach the molded handle, and remove the handle.
3. Remove the four 8-32 x 7/16" screws and shoulder washers from the back of the Monitor.
4. Remove the 8-32 x 1/4" screw from the back.
5. Remove the three 8-32 x 5/8" screws from the bottom of the Monitor.
6. Slide off the molded case. If necessary, start sliding the case by gently pushing against the fuse housing and host interface connector.
7. Remove the front panel dress nuts from the hose connectors.
8. Pull the bezel assembly away from the unit, initially lifting it away at the bottom until the flange is released from the top of the unit.
9. Disconnect the two ribbon cables from the system processor board (Figure 4-2).
10. Lift out the speaker assembly and disconnect the speaker cable.
11. Disconnect yellow, red, and blue color coded pneumatic tubes from the couplings at the top of the pneumatics board. Leave only the green coded tubing connected.
12. Lift up the pump foam mount flap, and lift the pump assembly out of the center housing. Disconnect the pump cable. Disconnect the muffler tubing at the suction connection to the pump, and remove the pump. Leave the check valve and hose connected to the pump pressure connection.

13. Remove the muffler tubing and muffler.

14. Pry off the retaining clips at either side of the unit.

15. Carefully slide the upper frame assembly from the lower frame.

16. Perform any additional disassembly that may be required for maintenance procedures.

3.14 REASSEMBLY PROCEDURES

1. Prepare the upper frame assembly for joining with the lower frame. Ensure that the display and keyboard assemblies are mounted on the upper case, and that their ribbon cables have been routed behind the display assembly. Ensure that the red color coded front panel hose connector tubing is installed and placed in the proper routing guide, as shown in Figure 4-2. Route the red coded tubing up behind the display assembly. Ensure that the blue coded front panel hose connector tubing is installed and placed in the proper routing guides, as shown in Figure 4-2. Route the blue coded tubing into the cavity in front of the pump cavity while ensuring that the tube remains in the routing guide under the upper frame.

2. Prepare the lower frame assembly for joining with the upper frame. Ensure that all circuit boards, fan assembly, and connectors have been installed as shown in Figure 3-3 and Figure 4-2. Connect the green color coded tubing from the sensor on the analog board to the green coded coupling on the pneumatics board. Ensure that the protective sleeve on this line is positioned at the cutout of the system processor board. Ensure that the tubing couplings of the pneumatics board are grouped closely together to allow the upper frame to pass around the pneumatics board when the two frames are joined.

3. Join the upper frame assembly to the lower frame, carefully positioning the circuit cards into the card guide slots as the two frames are joined together. Ensure that the blue coded tubing remains in the routing guide under the upper frame, and that the couplings at the pneumatics board remain closely grouped together, until the upper frame assembly is fully seated onto the lower frame assembly.

4. Attach the retaining clips that hold together the top and bottom assemblies.

5. If not already connected, install the check valve and short yellow coded tubing on the pump pressure coupling. Orient the check valve with the blue coded side toward the pump. Connect the pneumatics board yellow coded coupling to the pump tubing.

6. Install the pump mount foam into the pump cavity and place the pump into the foam as shown in Figure 4-2. Ensure the pump and mount are fully seated in the bottom of the cavity. Close the flap of the foam mount over the pump and around the pump tubing.

7. Install the pump cable connector at the top of the pneumatics board.

8. Connect the red coded coupling to the red coded tubing.

9. Connect the blue coded coupling to the blue coded tubing.

10. Pass the muffler tubing through the opening at the right side of the unit, and thread the tubing up past the power supply board. Continue to thread the tubing into the top of the frame assembly, past the edge of the power supply board, and into the middle cavity near the top of the pneumatics board, as shown in Figure 3-4.

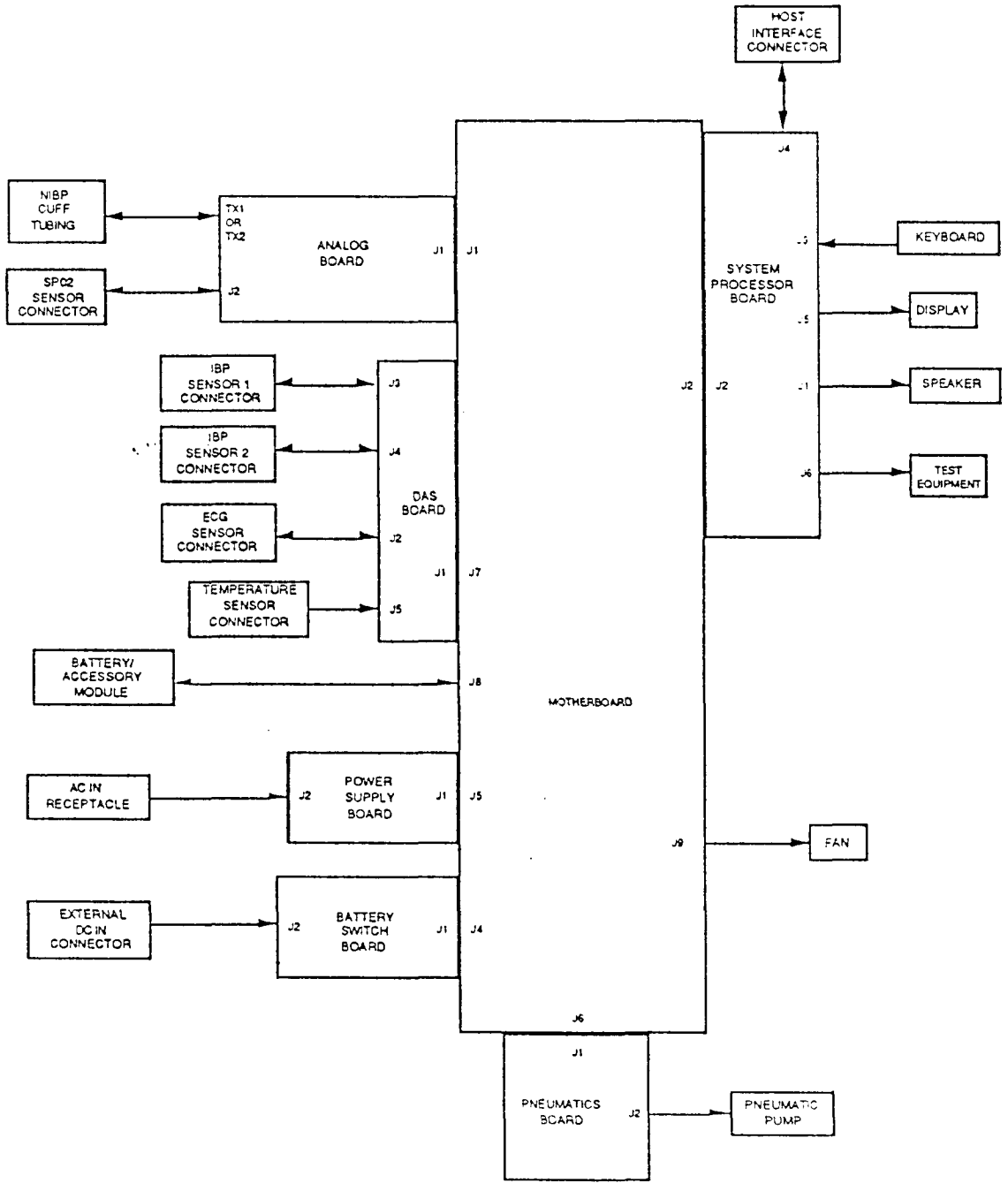


Figure 3-3. Model 8720 Interconnection Diagram

11. Connect the muffler tubing to the pump suction coupling.

12. Connect the speaker cable connector at the top of the system processor board.

13. Install the speaker assembly in the top of the pump cavity, inserting the tab into the rear of the frame and snapping down the front end. Ensure that the two pump tubes are routed freely through the openings at either side of the speaker assembly front edge.

14. Taking up any slack in the muffler tubing, place the muffler inside the unit opening, as shown in Figure 4-2.

15. Connect the display and keyboard ribbon cable connectors to the receptacles in the system processor board, and tuck the cables behind the speaker assembly clamp bar. Press down the bar.

16. Install the bezel assembly, inserting the top edge into the unit flange before placing the bezel assembly on front of the unit.

17. Fasten the bezel assembly by installing the two front panel dress nuts on the hose connectors. Use finger pressure to tighten the nuts.

18. Slide the molded case onto the unit.

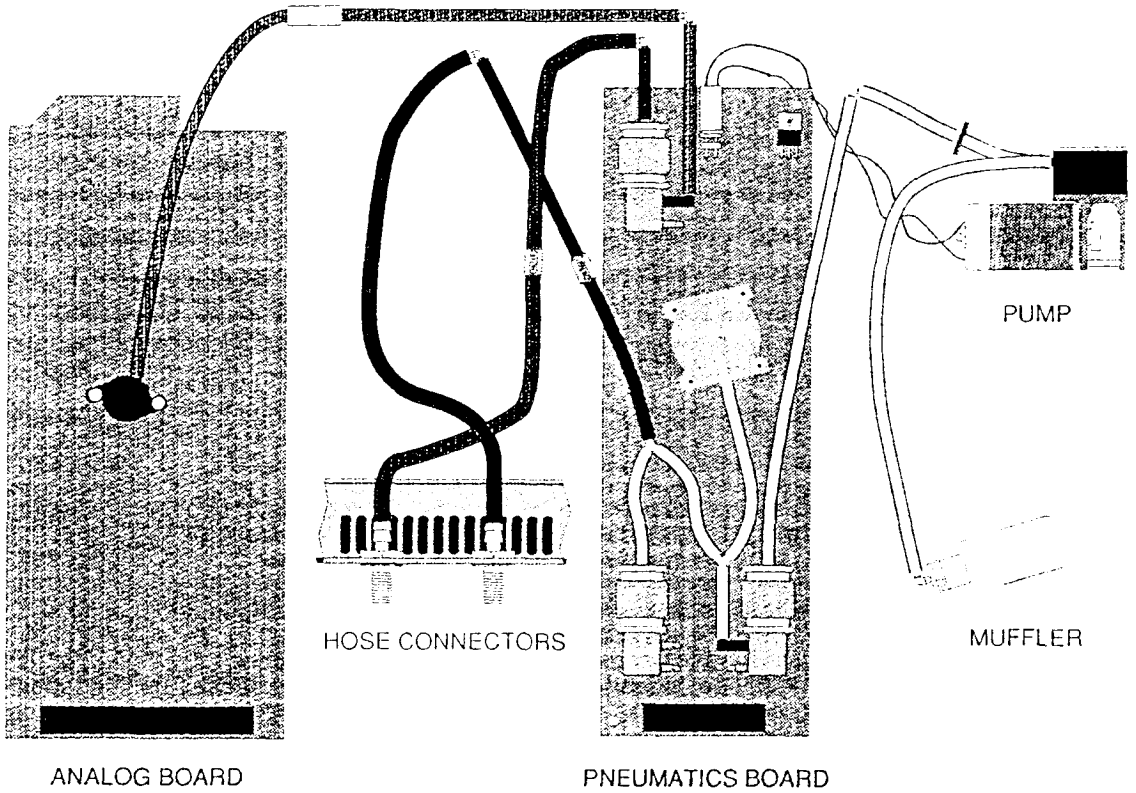
19. Install the 8-32 x 1/4" screw at the rear of the molded case.

20. Install the four 8-32 x 7/16" screws and shoulder washers at the rear of the case

21. Install the three 8-32 x 5/8" screws at the bottom of the Monitor.

22. Attach the molded handle using the two handle fasteners.

23. Attach the access plate (or accessory module) using the 1/4-20 x 5/8" screw.



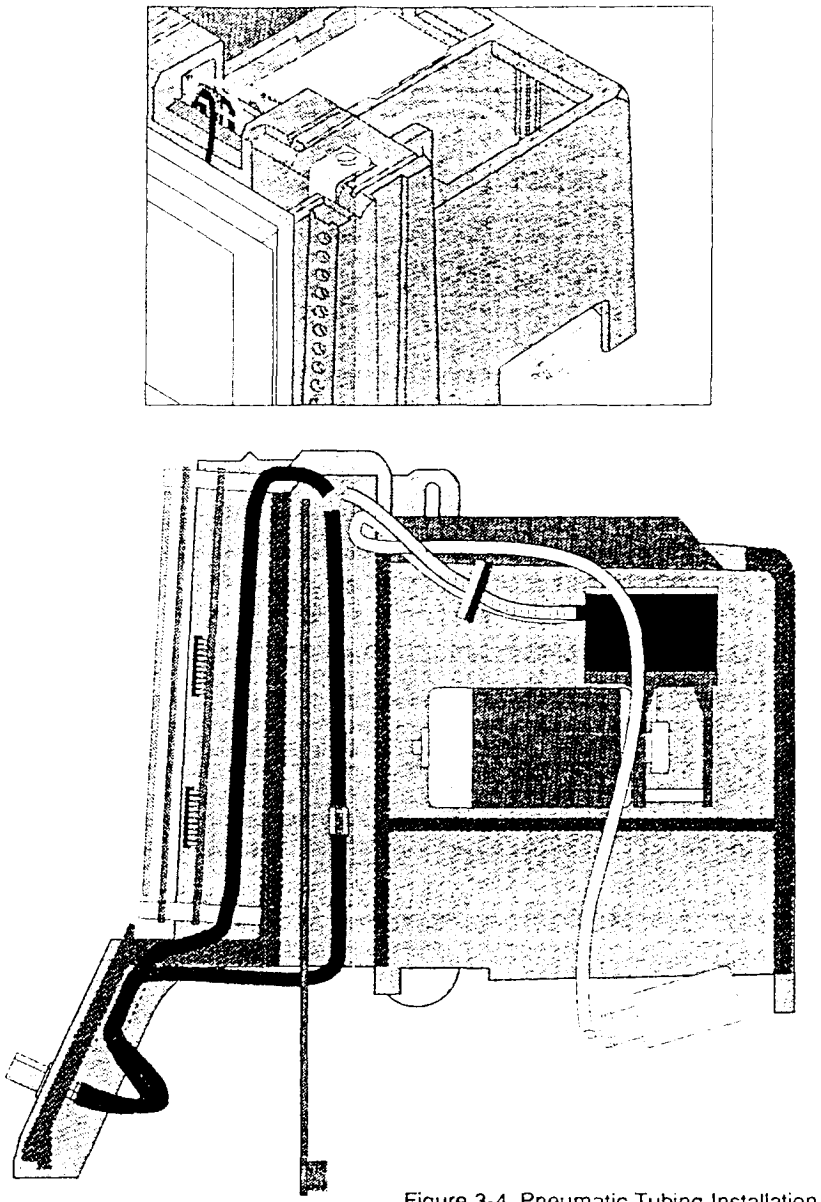


Figure 3-4. Pneumatic Tubing Installation

SECTION 4. SERVICE DIAGRAMS & PARTS LISTS

4.1 INTRODUCTION

This section of the manual provides the parts lists, component drawings, and service diagrams necessary to maintain the equipment and to order replacement parts.

The component drawings follow the parts lists. The following illustrations are contained in this section:

FIGURE NUMBER	FIGURE TITLE
4-1	Top Assembly
4-2	Sub-Top Assembly

4.2 LIST OF APPLICABLE SERVICE DIAGRAMS

An alphabetical listing of the service diagrams contained in this manual at the time of publication is provided below. The service diagrams appear in schematic number order in the back of this section.

BOARD TITLE & NO.	SCHEMATIC NUMBER
Analog Board (315-334)	SC315-334 PC (4 sheets)
Battery Switch Board (315-371)	SC315-371 PB (2 sheets)
DAS Board (315-370)	SC315-370 PD (5 sheets)
Motherboard (315-373)	SC315-373 PA (1 sheet)
Pneumatics Board (315-376)	SC315-376 PA (1 sheet)
Power Supply Board (315-367)	SC315-367 PB (3 sheets)
System Processor Board (315-332)	SC315-332 PB (8 sheets)

TOP ASSEMBLY PARTS LIST

(Refer to Figure 4-1)

ITEM	DESCRIPTION	PART NUMBER
1	Case, Molded	759-246
2	Handle, Molded	759-245
3	Plate, Access	704-731
4	Fastener, Handle	704-732
5A	Overlay, Connectors 008720	701-328
5B	Overlay, Connectors 008710	701-343
6	Screw, 8-32 x 5/8" pnh phh sst	719-199
7	Screw, 8-32 x 1/4" trusshd ph sst	722-164
8	Screw, 8-32 x 7/16" trusshed ph sst	722-171
9	Screw, 1/4-20 x 5/8" pnh ph sst	719-269
10	Nut, Front Panel Dress	704-742
11	Washer, Shoulder, Pole Clamp	748-291
12	Bumper Black .5 square, .12 high	732-161
13	Bezel Assembly	332-201
14	Sub-Top Assy	351-062
15	Label, Operating Precaution (left side)	730-930
16	Label, Operating Precaution (right side)	730-931
17	Label, CSA Caution/Warning (English)	730-932
18	Label, Fuse Warning (Domestic)	728-158
19	Label, Model Number	728-159
20	Label, CSA Caution/Warning, (French)	730-933
21	Label, Serial Number	728-153

SUB-TOP ASSEMBLY PARTS LIST

(Refer to Figure 4-2)

ITEM	DESCRIPTION	PART NUMBER
1	**Lower Frame Assembly**	336-085
1A	PWA, Analog (w/ 622-151 Xducer)	315-334
1B	PWA, Power Supply	315-367
1C	PWA, System Processor	315-332
1D	PWA, Pneumatics, MPL SW.	315-376
1E	PWA, Battery Switch	315-371
1F	PWA, Data Acquisition System	315-370
1G	PWA, Motherboard	315-373
1H	Frame, Lower	759-248
1I	Connector Plate Assembly	320-539
1J	Rivet, Snap Black Nylon	727-148
1K	External DC Assembly	320-546
1L	Power Entry Assembly	320-547
1M	Fan Assembly	320-565
1N	Rivet, Snap, SR4100	727-149
1O	Muffler Assembly	320-397
1P	Tubing, OD .250, ID .125	740-107
2	**Upper Frame Assembly**	336-086
2A	Frame, Upper	759-251
2B	Cuff Port	704-807
2C	Nut, Hex Special, 5/16-24 Brass	715-117
2D	Filter, Air, 43 Micron Stainless	754-136
2E	Tubing, OD .250, ID .125	740-107
2F	Display Assembly	320-537
2G	Keyboard Assembly	320-538
2H	Rivet, Snap Black Nylon	774-148
2I	Tape, Wire Marker, Red	774-153
2J	Tape, Wire Marker, Blue	774-155
2K	Adhesive, Low Strength (Cyano)	782-160
3	Clip, Symmetric C-Type	736-182
4	Foam, Pump Mount	750-171
5	Speaker Housing Assembly	320-535
6	Pump Assembly	320-536

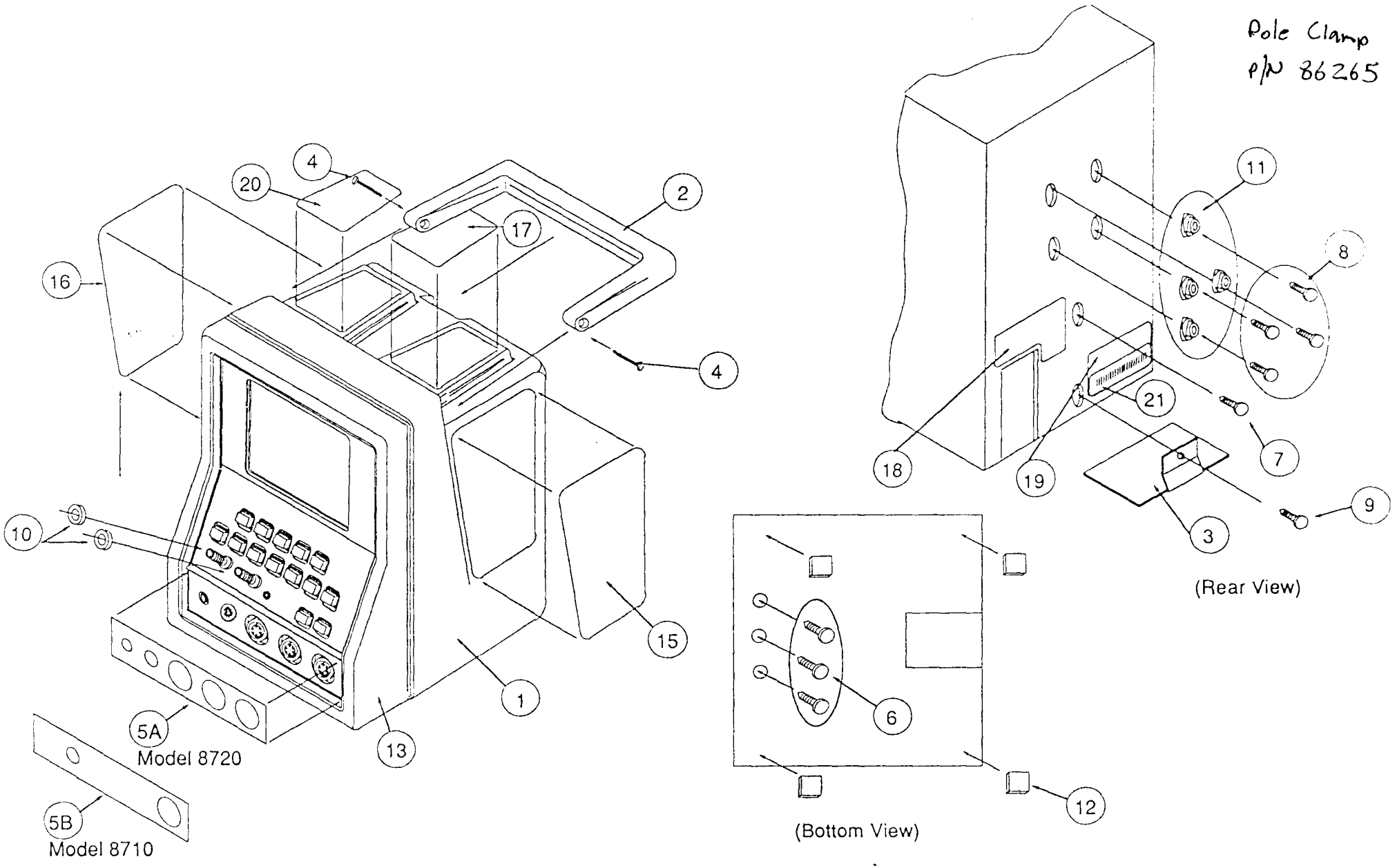
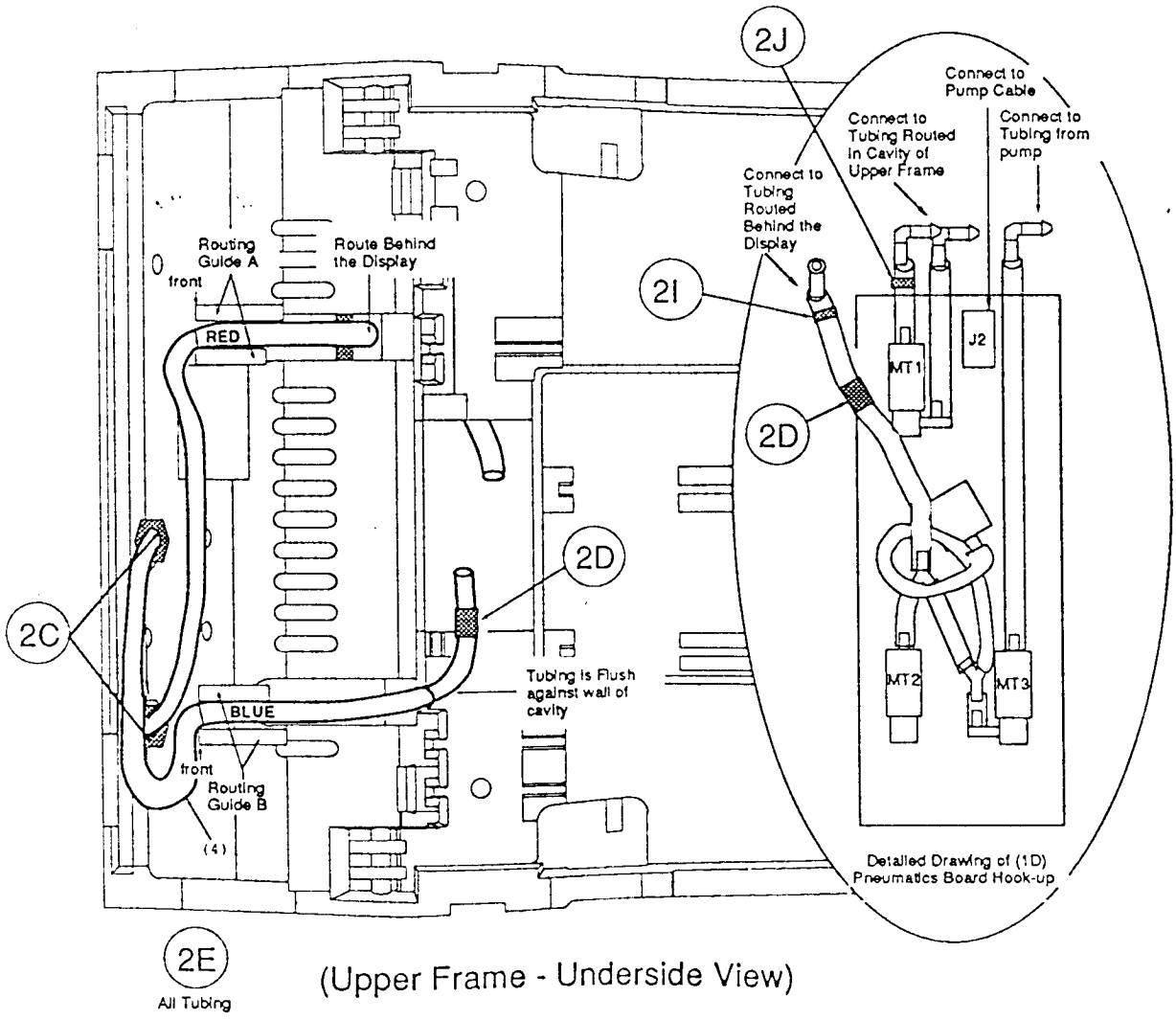


Figure 4-1. Top Assembly


2J
Connect to Pump Cable
Connect to Tubing Routed in Cavity of Upper Frame
Connect to Tubing from pump
Connect to Tubing Routed Behind the Display
2I
J2
MT1
2D
Routing Guide A
front
Route Behind the Display
RED
2D
2C
Tubing is Flush against wall of cavity
MT2
MT3
BLUE
front
Routing Guide B
(4)
Detailed Drawing of (1D) Pneumatics Board Hook-up
2E
All Tubing
(Upper Frame - Underside View)

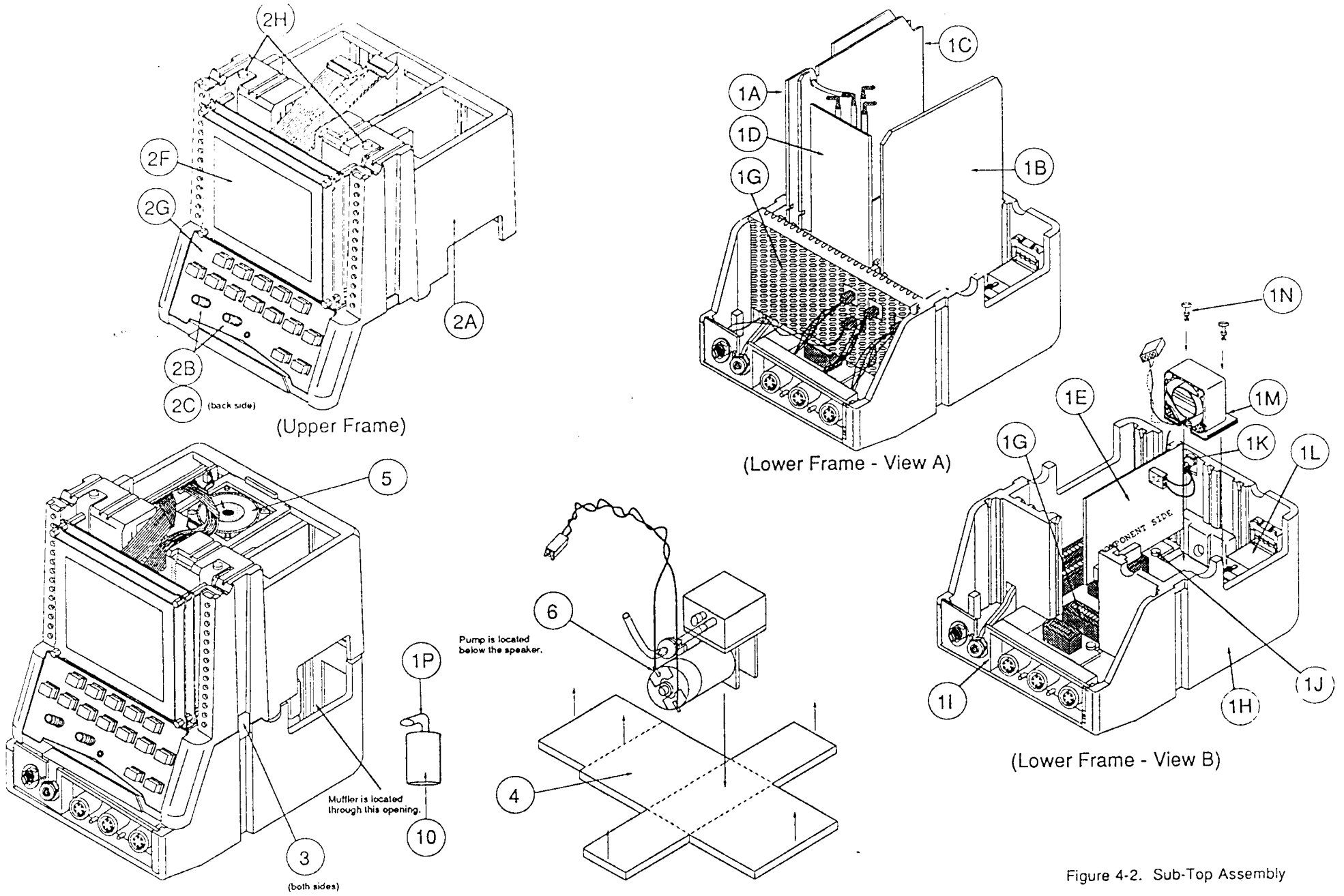
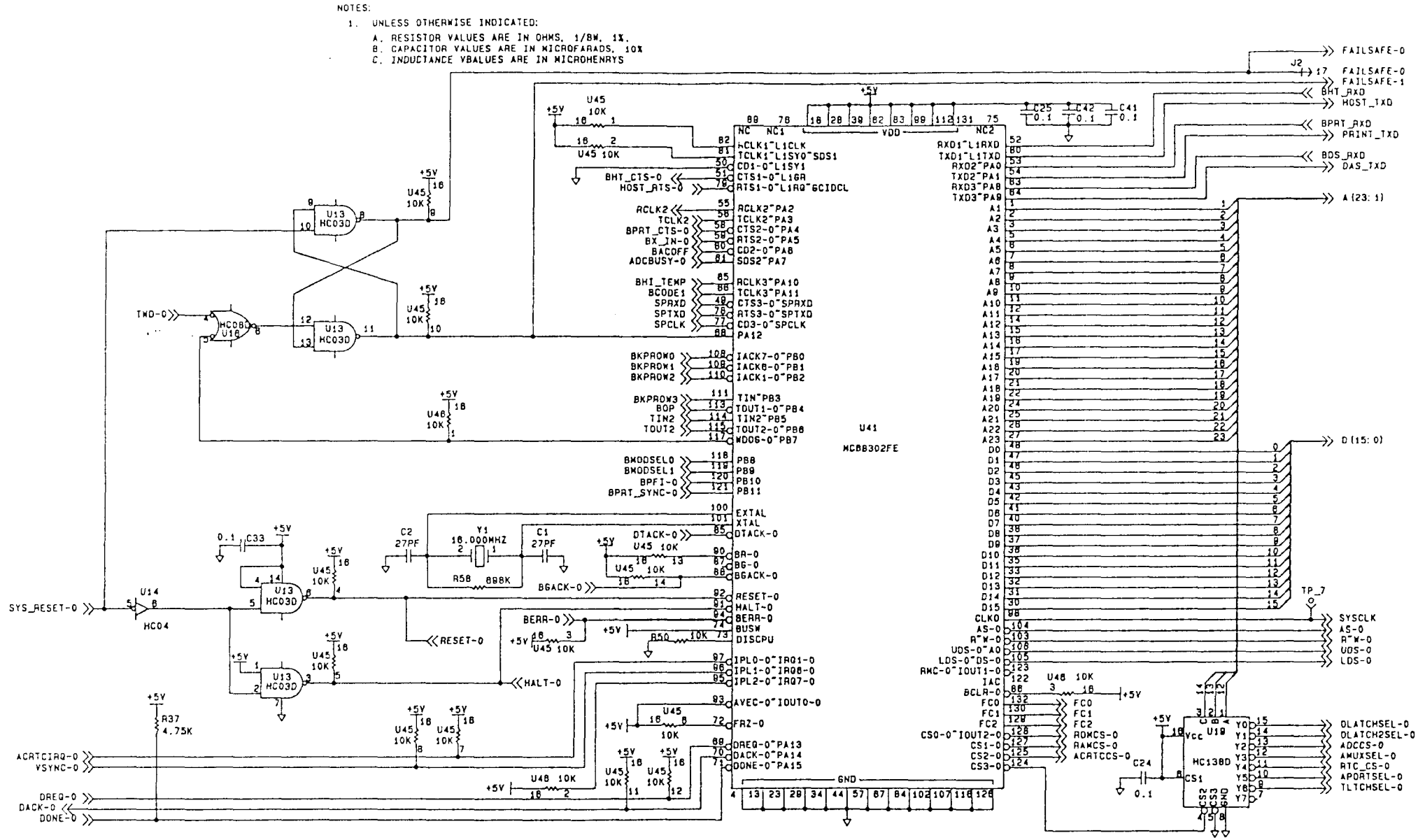
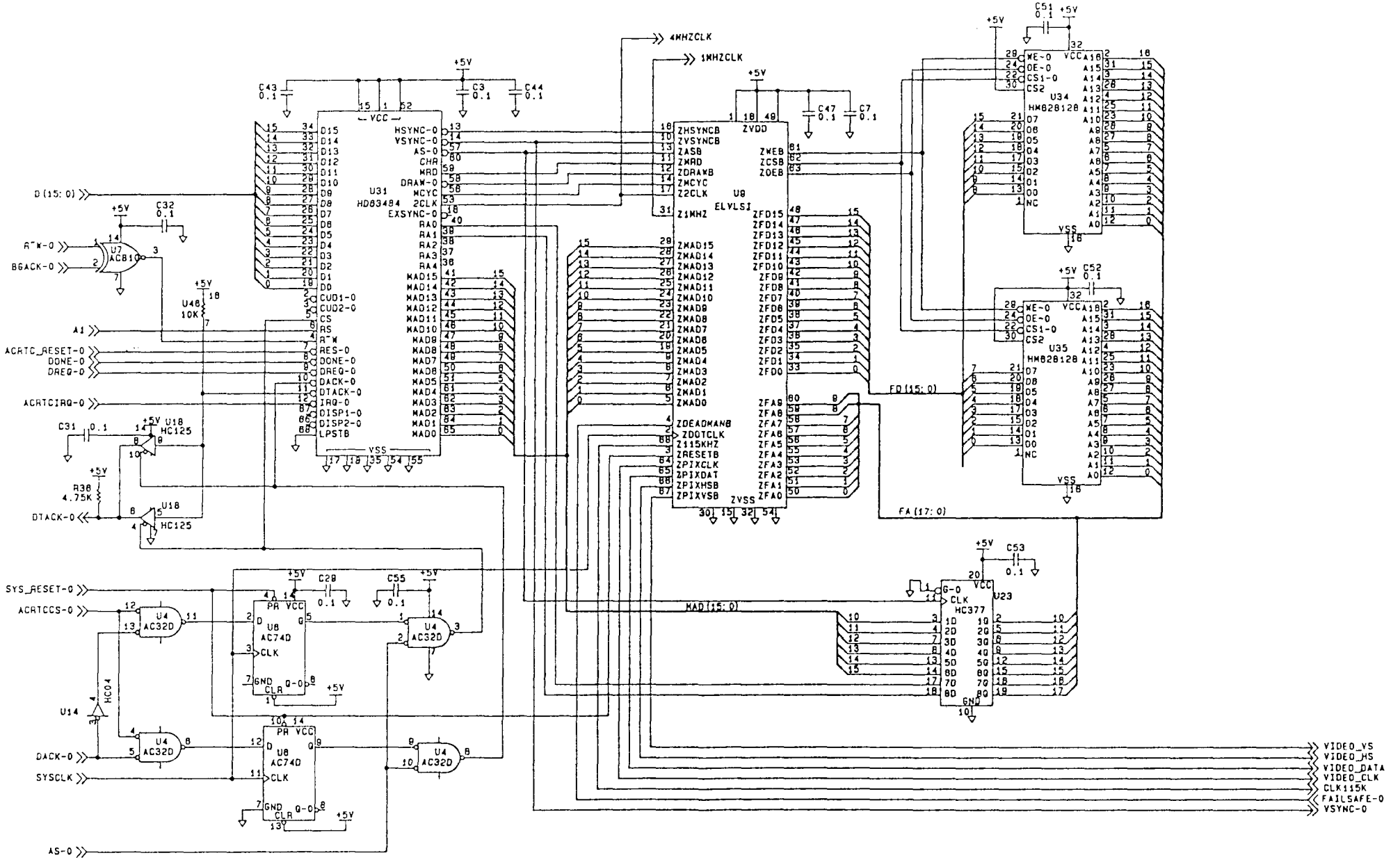


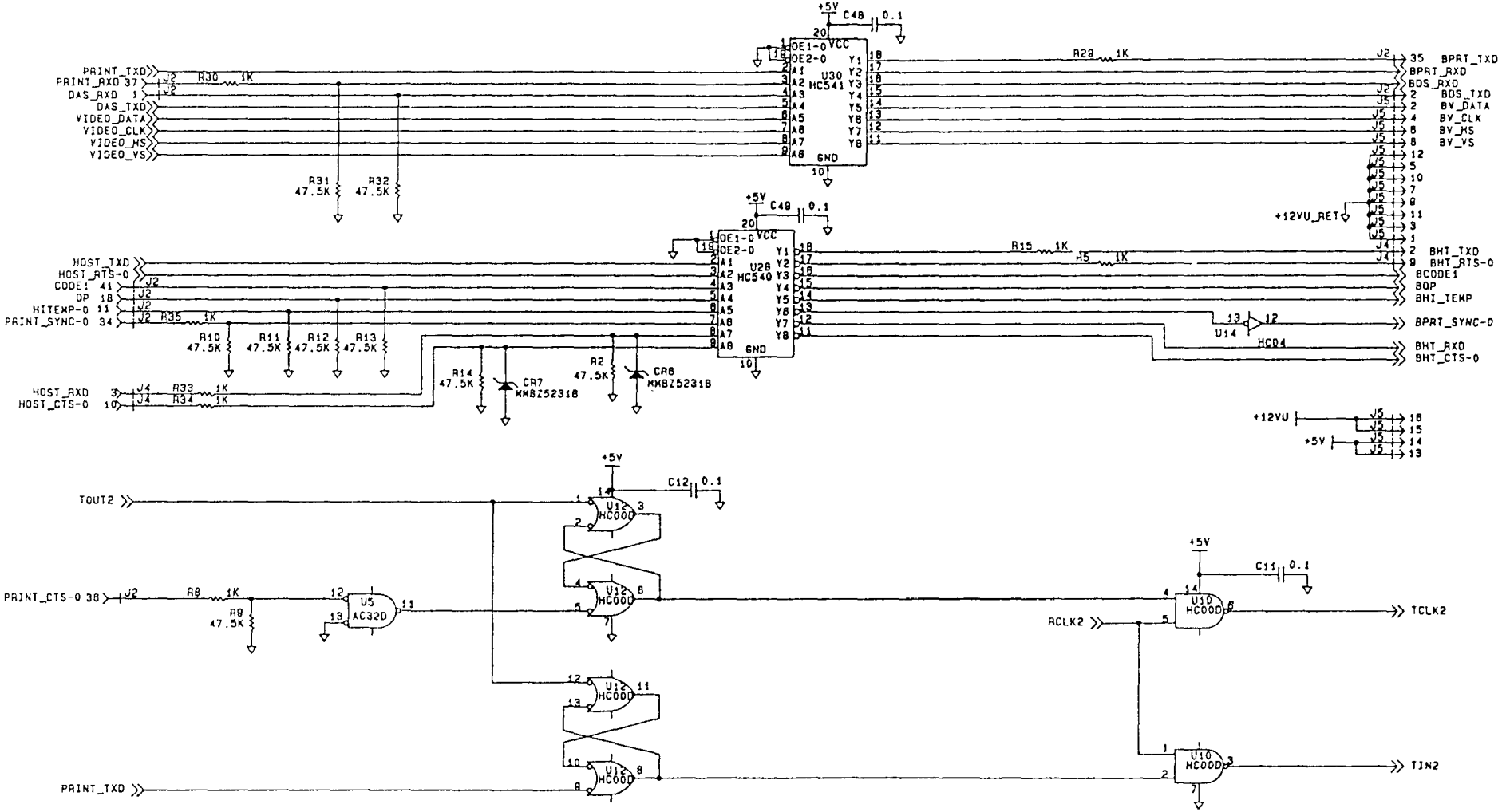
Figure 4-2. Sub-Top Assembly



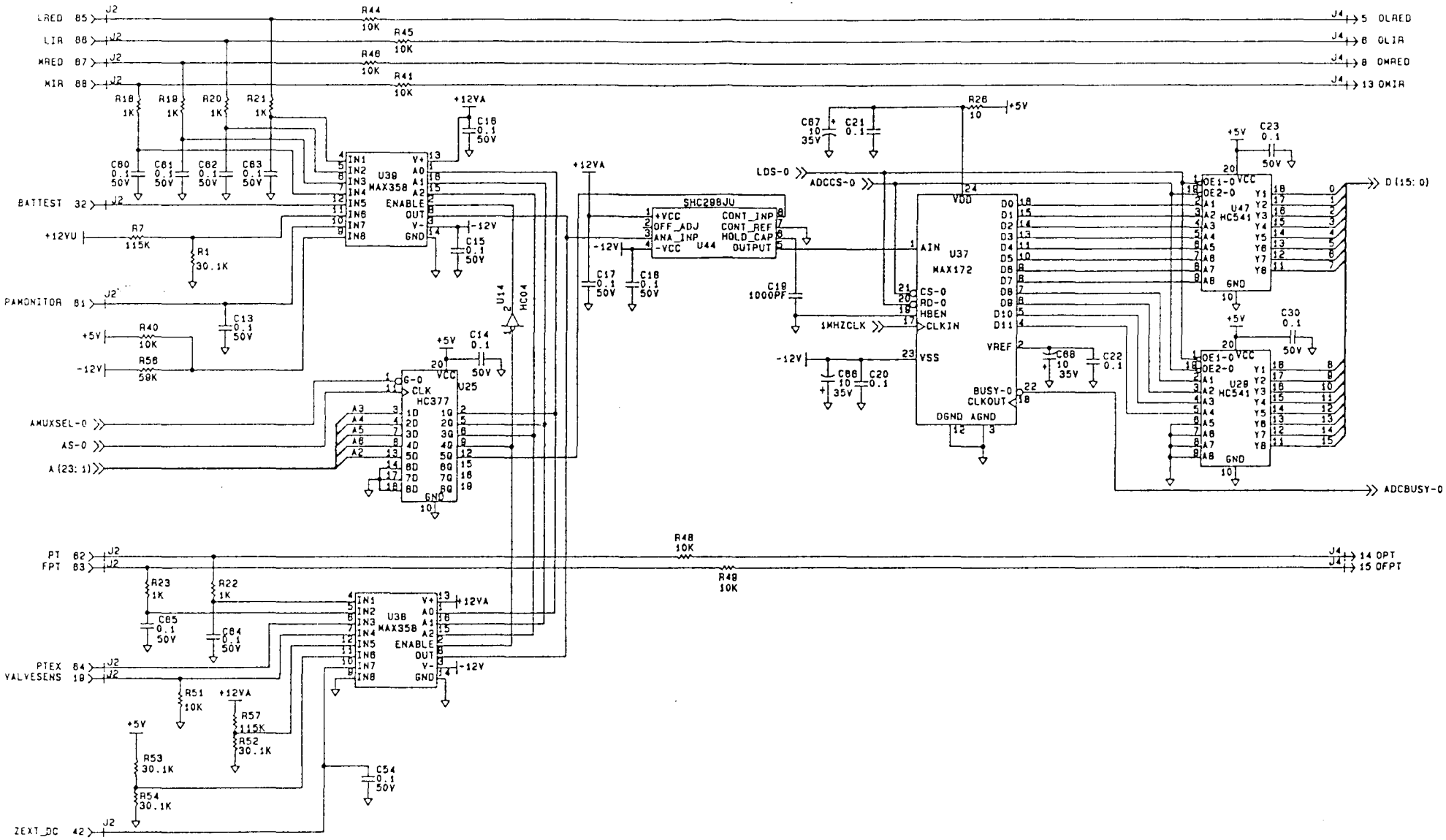
SC315-332 PB
System Processor Board Schematic (1 of 8)



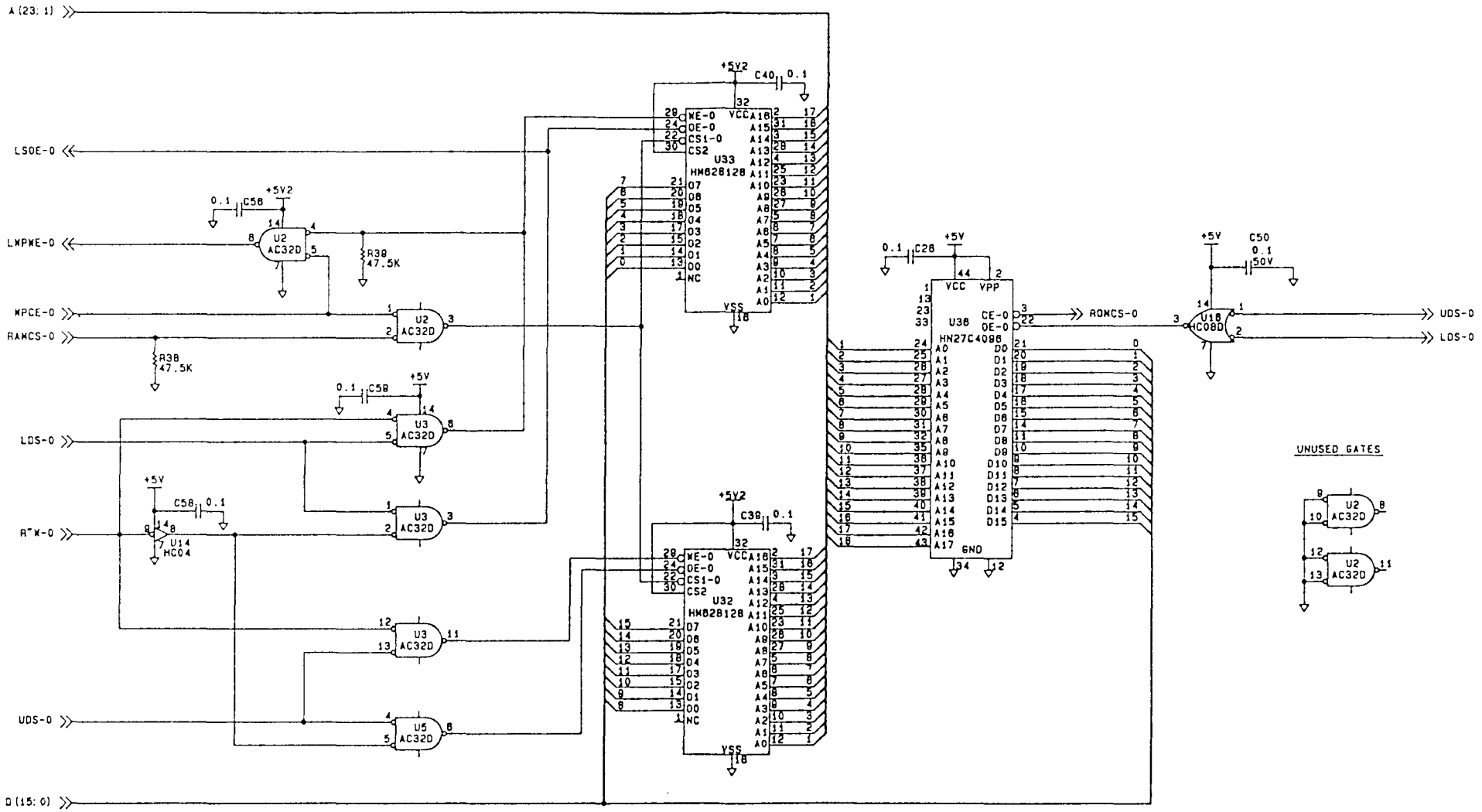
SC315-332 PB
System Processor Board Schematic (2 of 8)



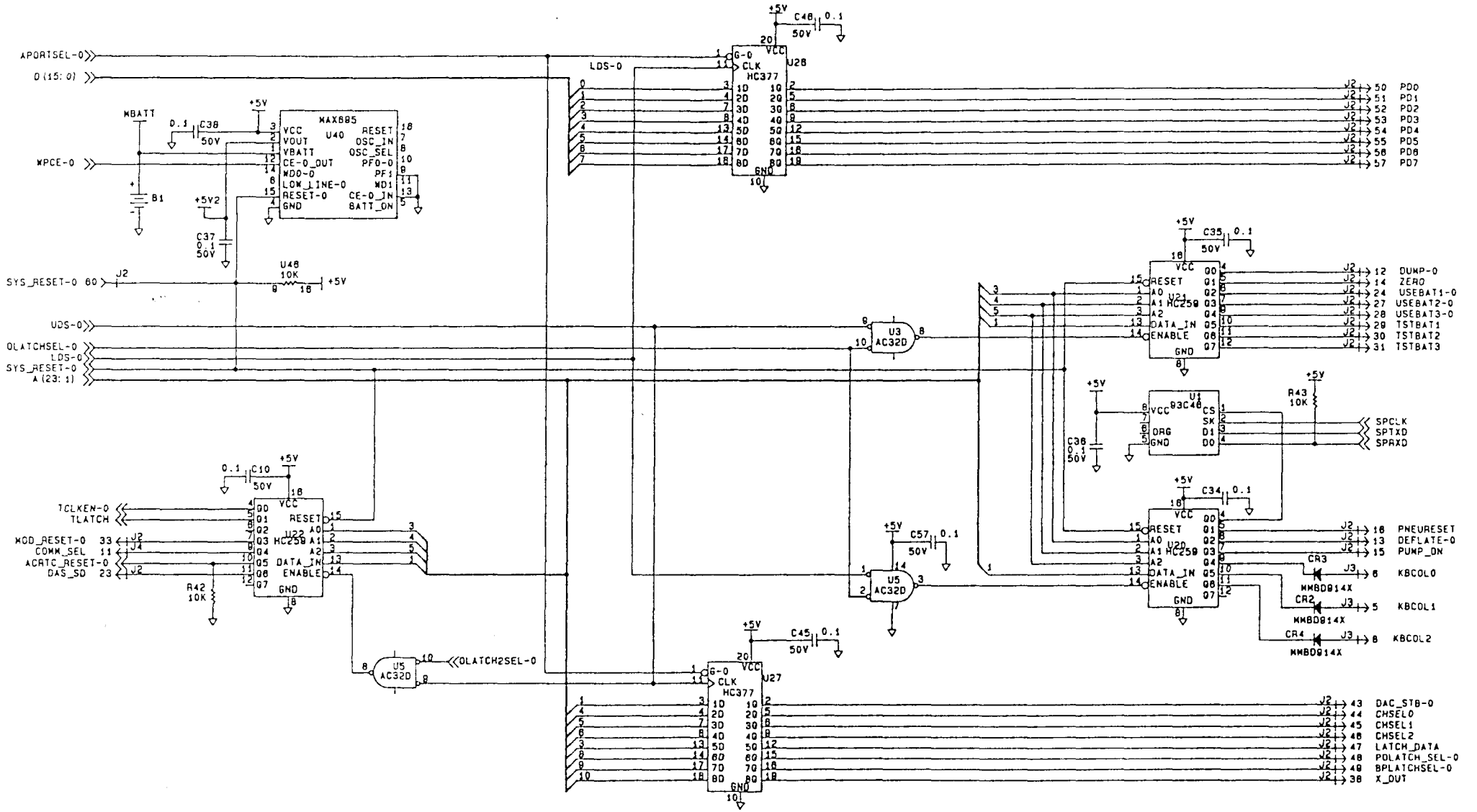
SC315-332 PB
System Processor Board Schematic (3 of 8)



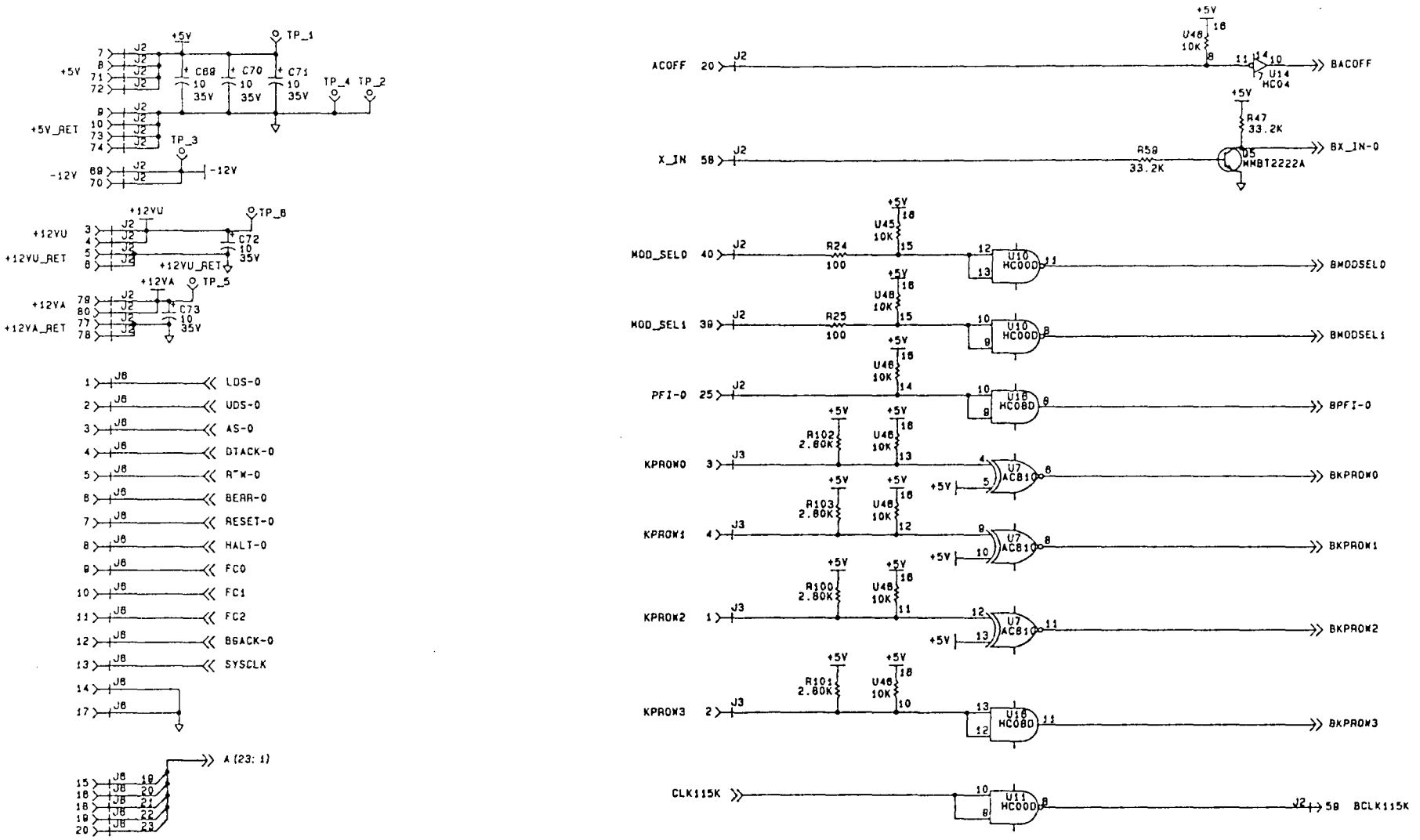
SC315-332 PB
System Processor Board Schematic (4 of 8)



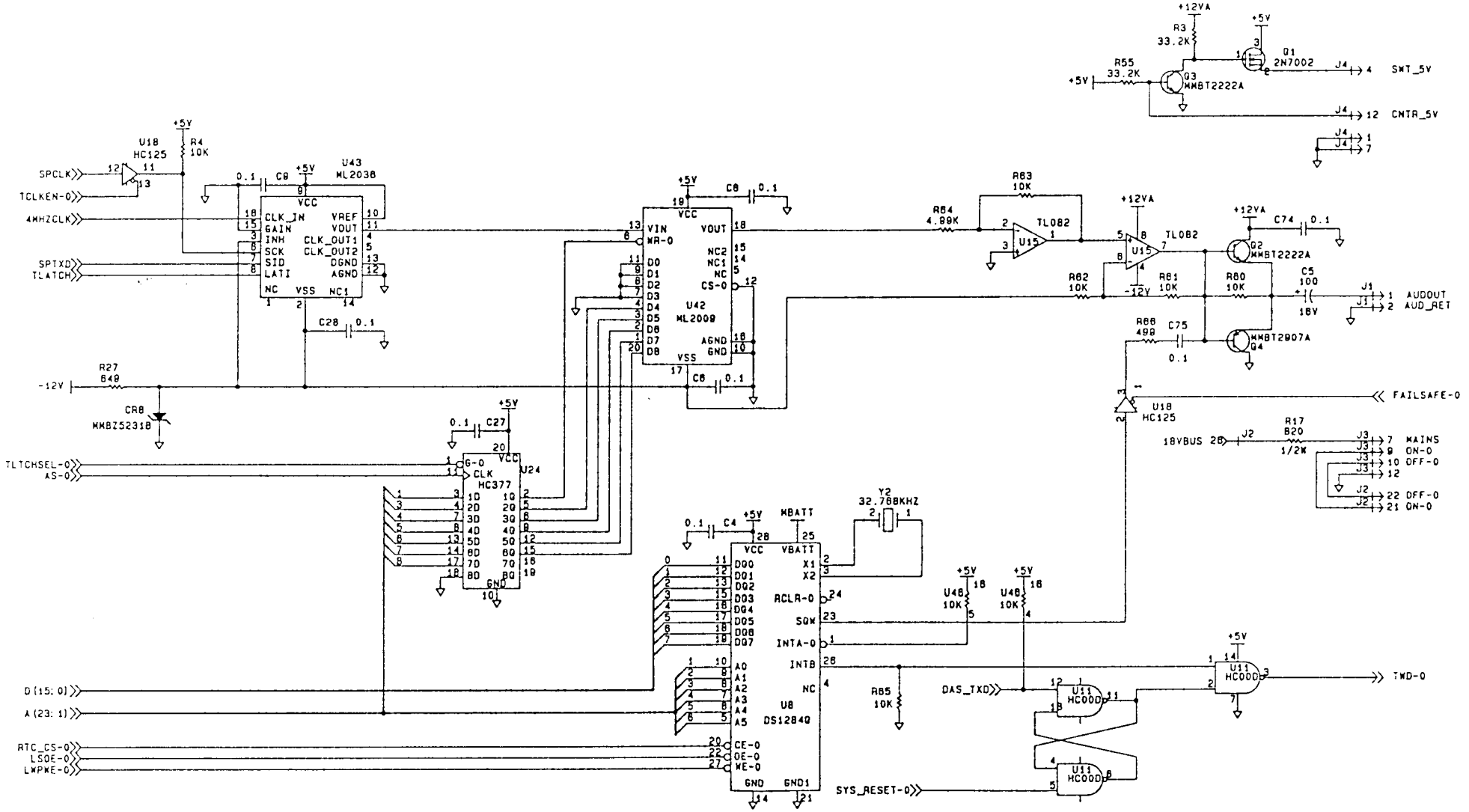
SC315-332 PB
System Processor Board Schematic (5 of 8)



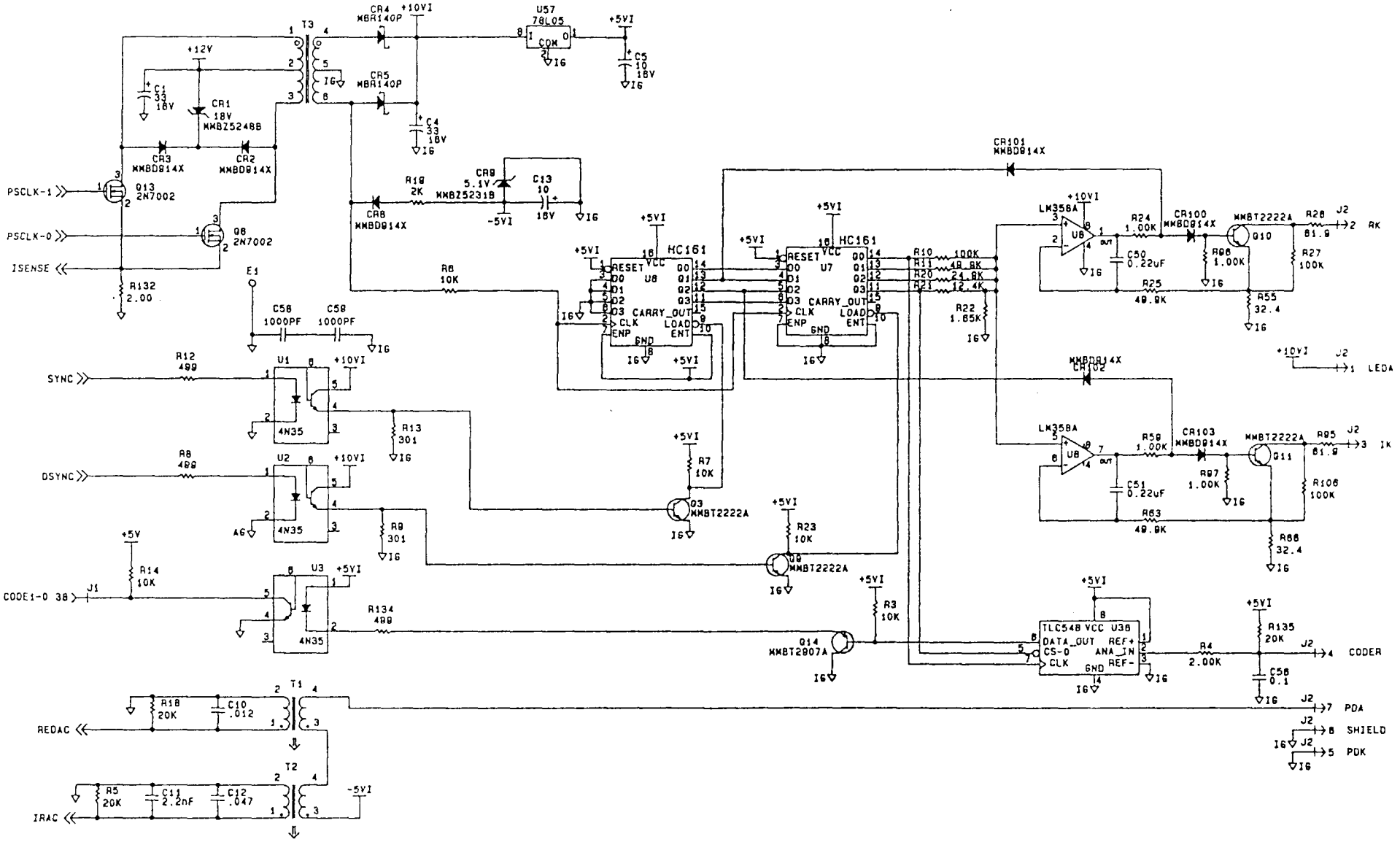
SC315-332 PB
System Processor Board Schematic (6 of 8)



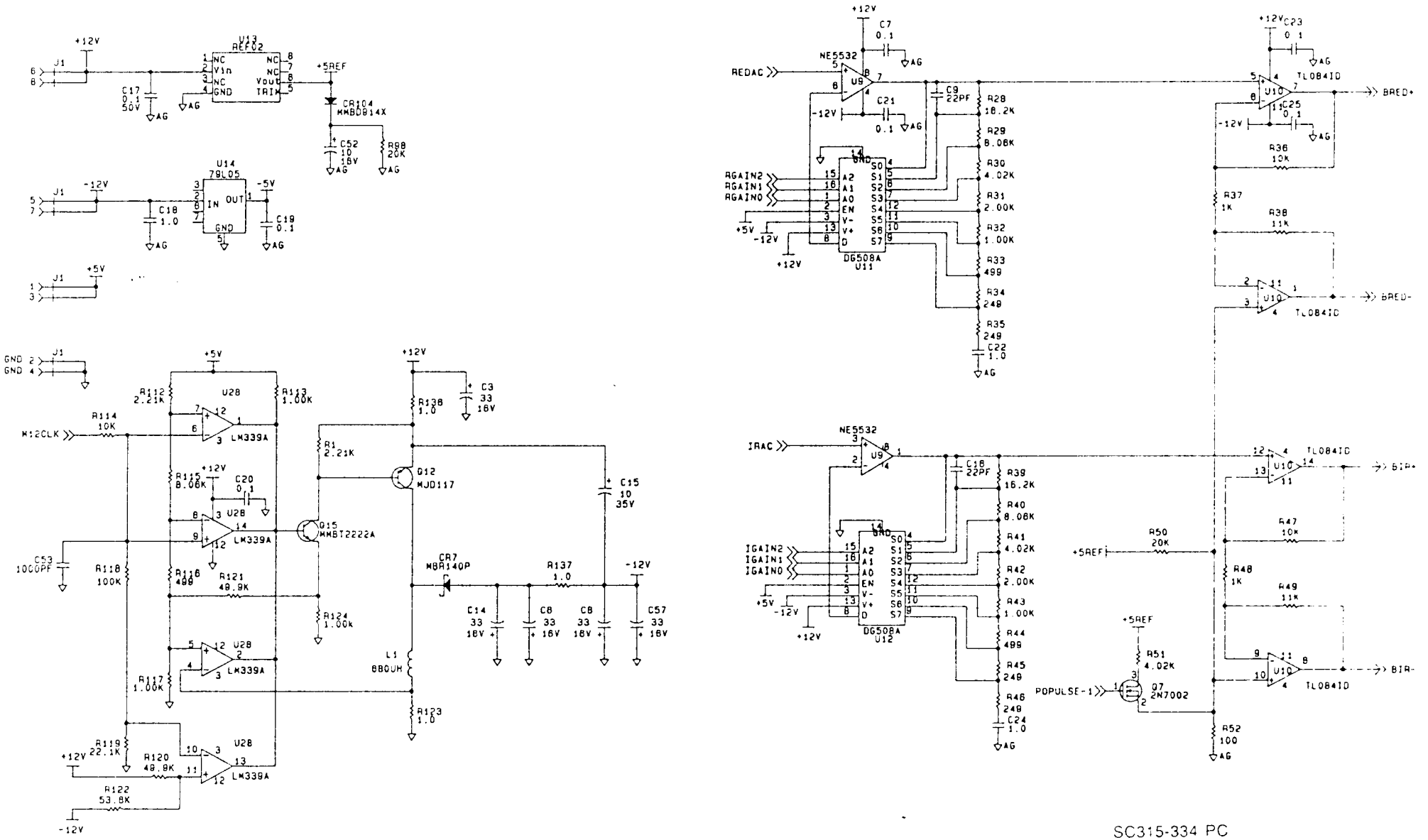
SC315-332 PB
System Processor Board Schematic (7 of 8)



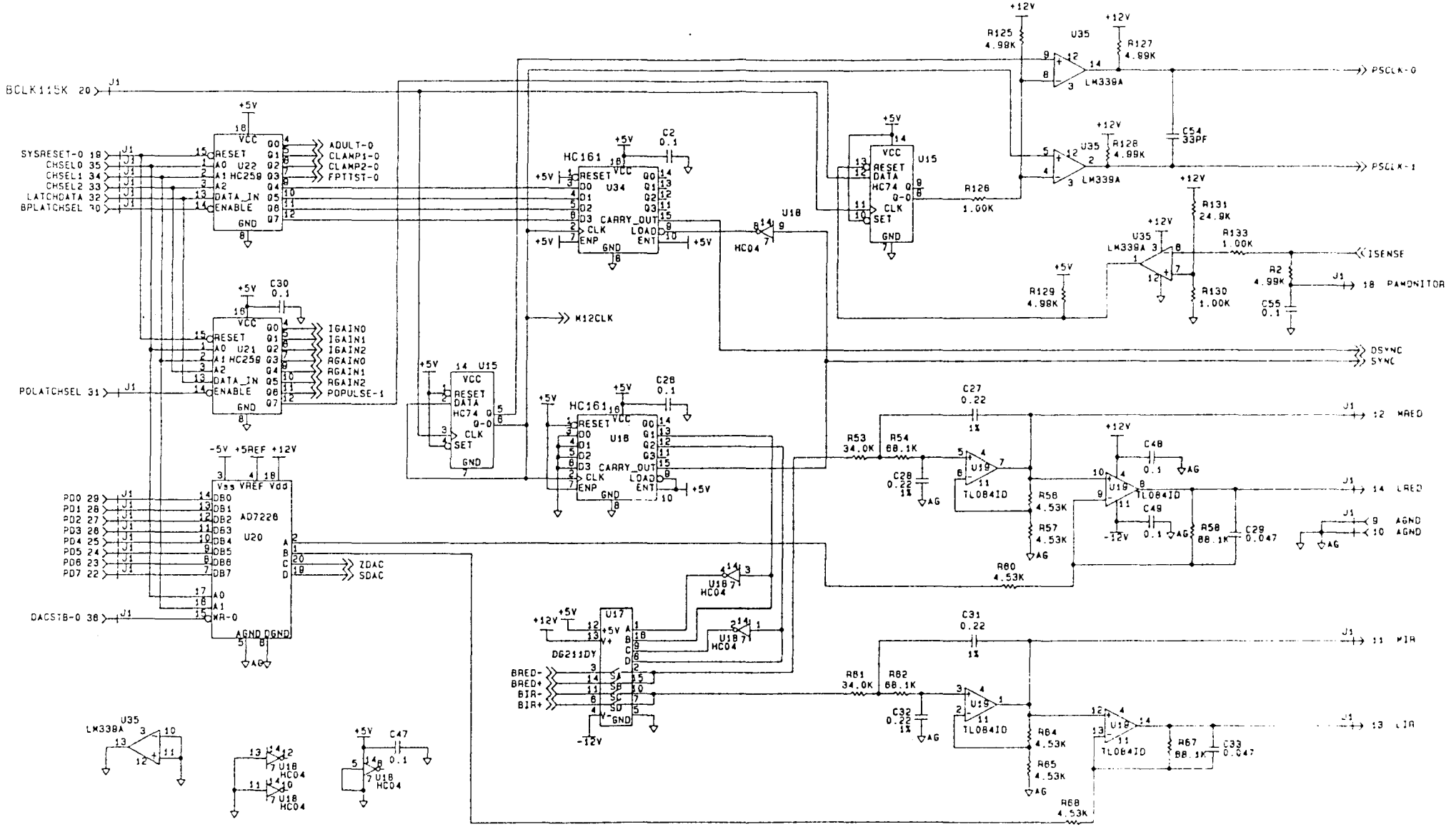
SC315-332 PB
System Processor Board Schematic (8 of 8)



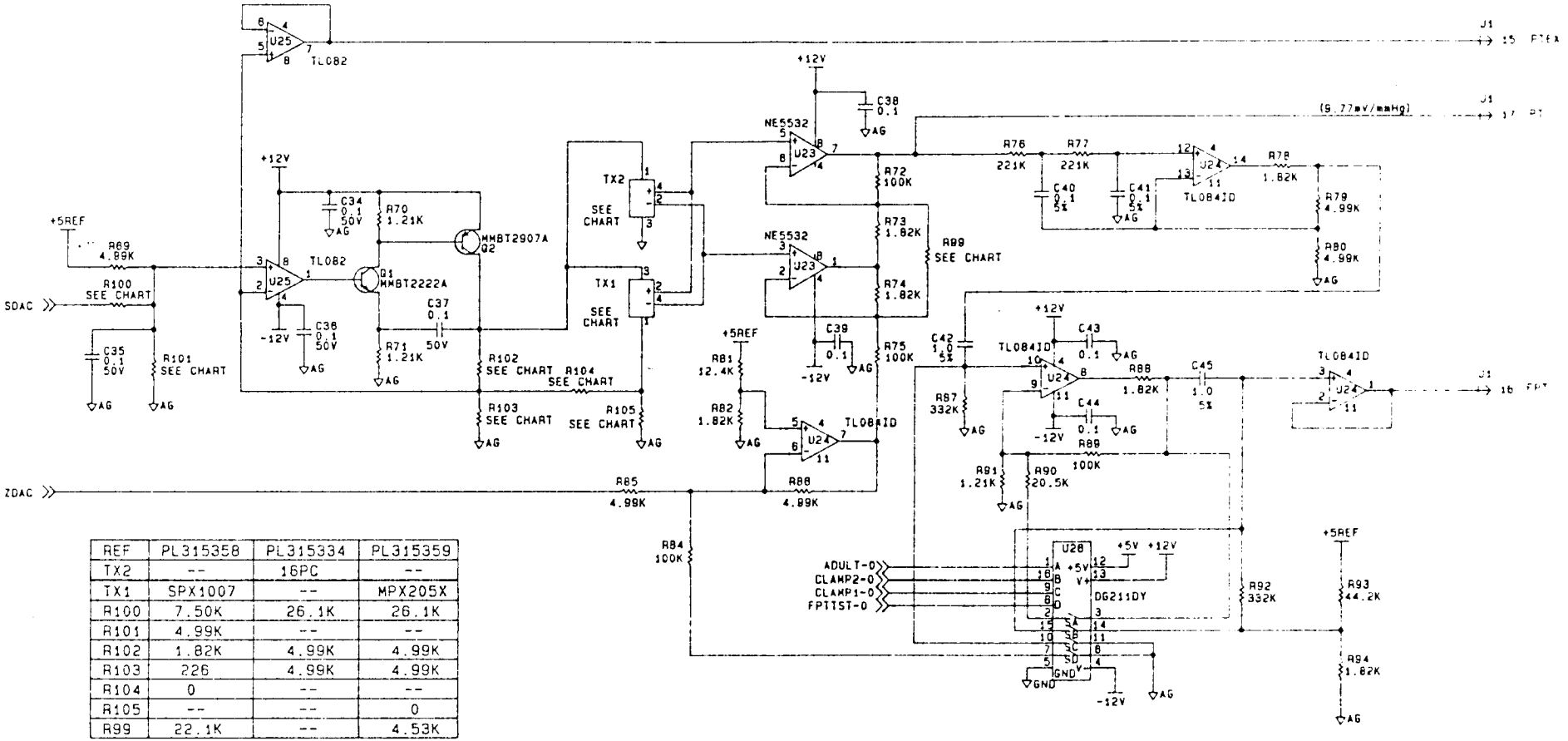
SC315-334 PC
Analog Board Schematic (1 of 4)



SC315-334 PC
Analog Board Schematic (2 of 4)

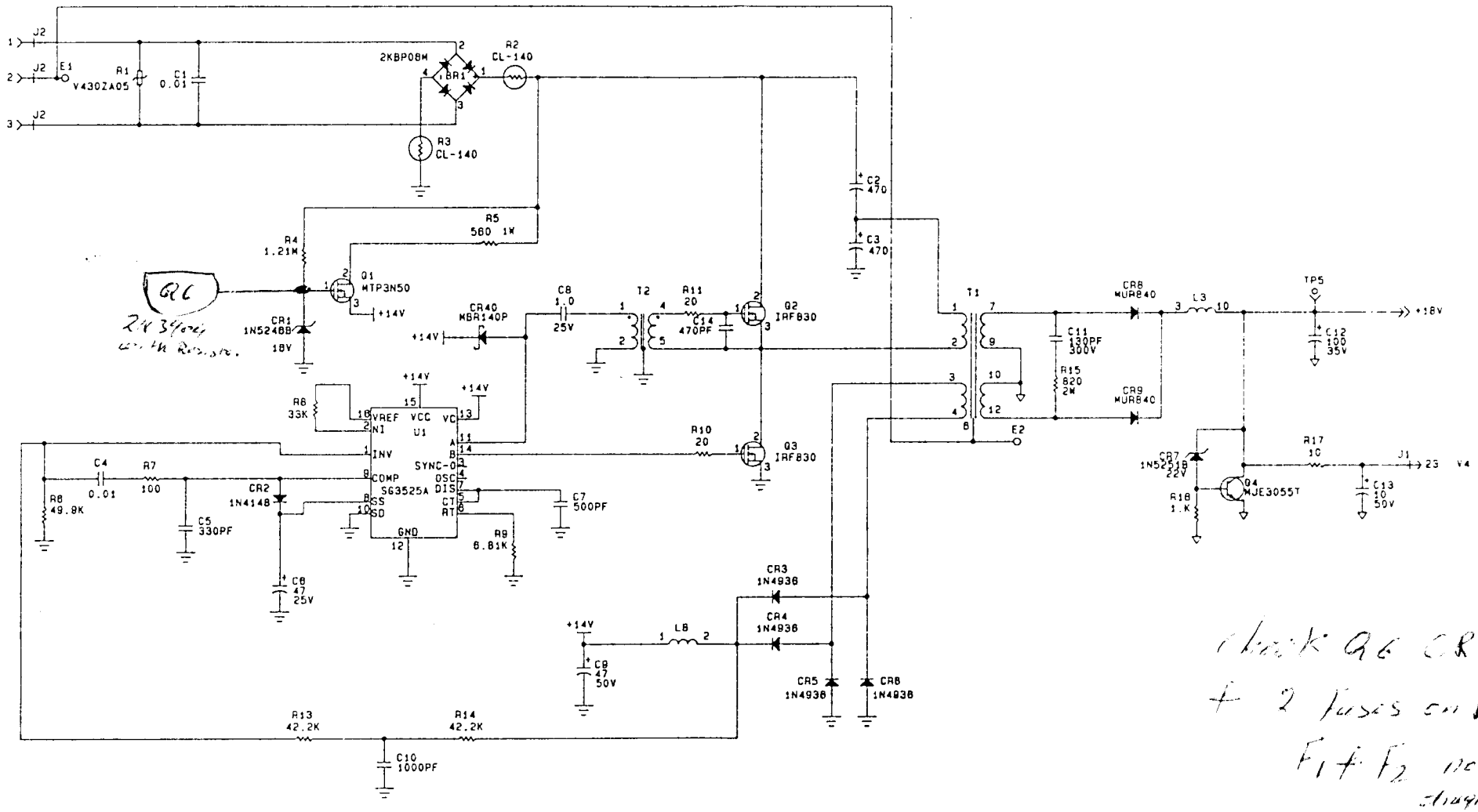


SC315-334 PC
Analog Board Schematic (3 of 4)



REF	PL315358	PL315334	PL315359
TX2	--	16PC	--
TX1	SPX1007	--	MPX205X
R100	7.50K	26.1K	26.1K
R101	4.99K	--	--
R102	1.82K	4.99K	4.99K
R103	226	4.99K	4.99K
R104	0	--	--
R105	--	--	0
R99	22.1K	--	4.53K

SC315-334 PC
Analog Board Schematic (4 of 4)



QC

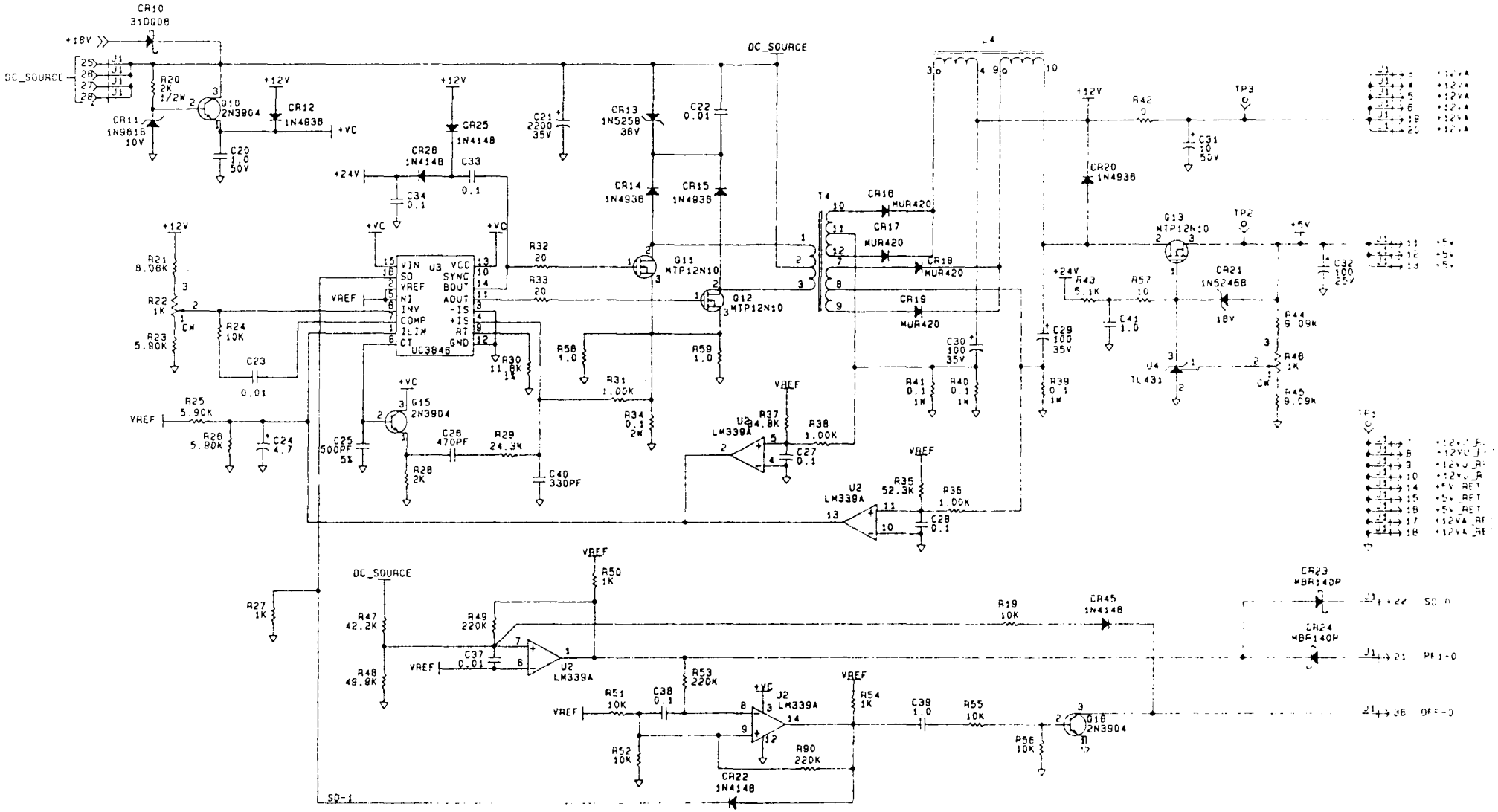
2N3904 with Resistor.

check Q6 CR1

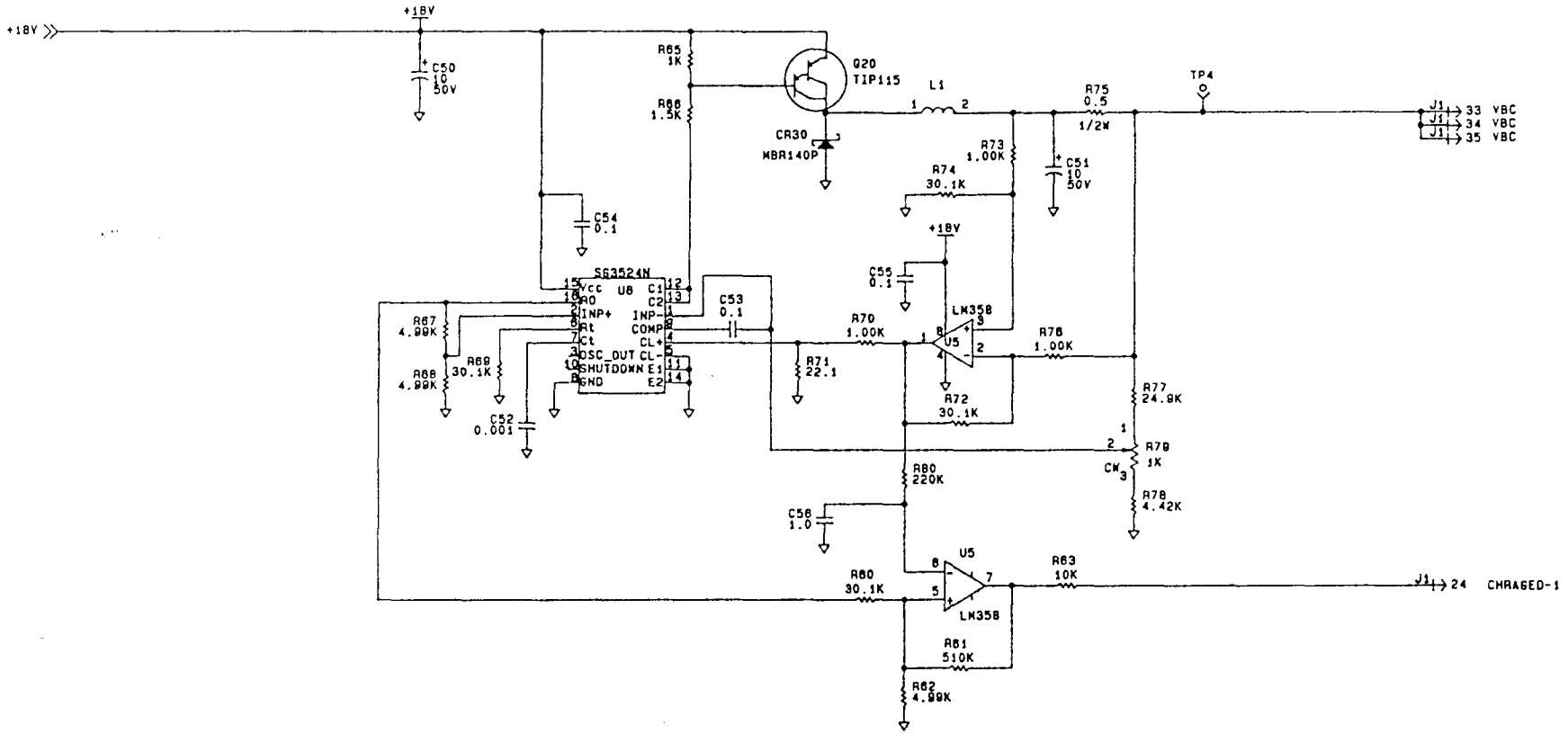
+ 2 fuses on board 2A

F1 + F2 not on this diagram.

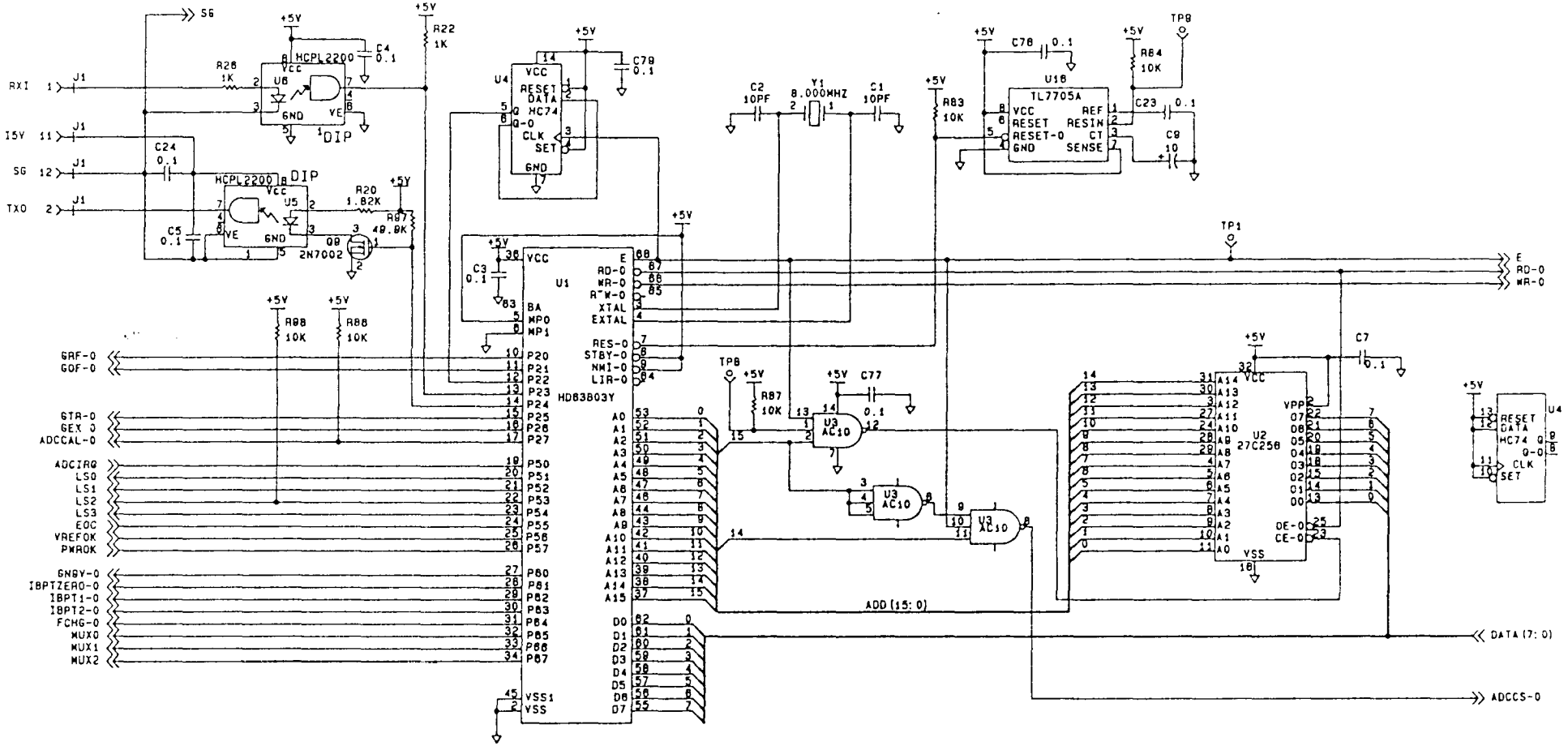
SC315-367 PB
Power Supply Board Schematic (1 of 3)



SC315-367 PB
Power Supply Board Schematic (2 of 3)



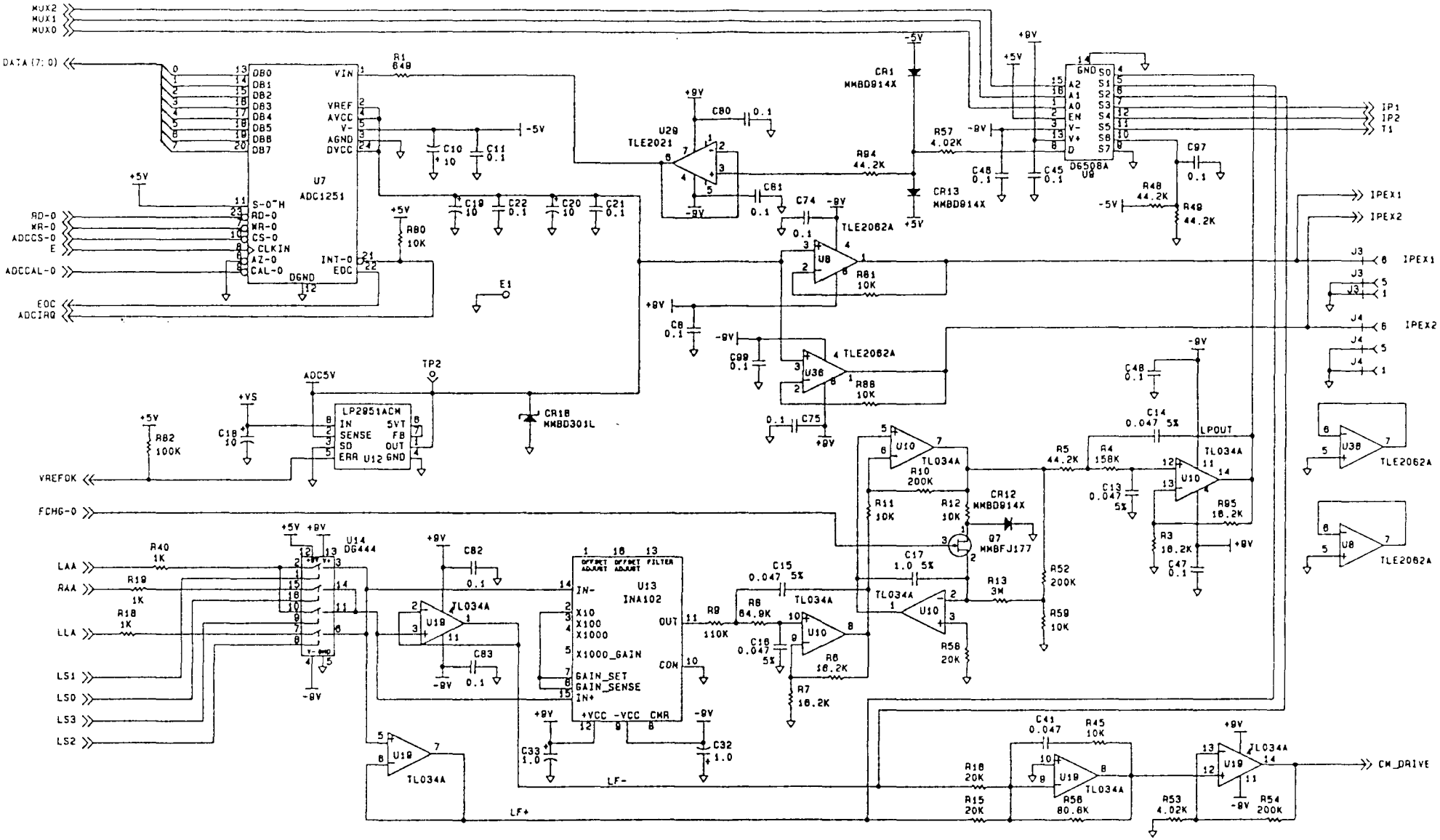
SC315-367 PB
Power Supply Board Schematic (3 of 3)



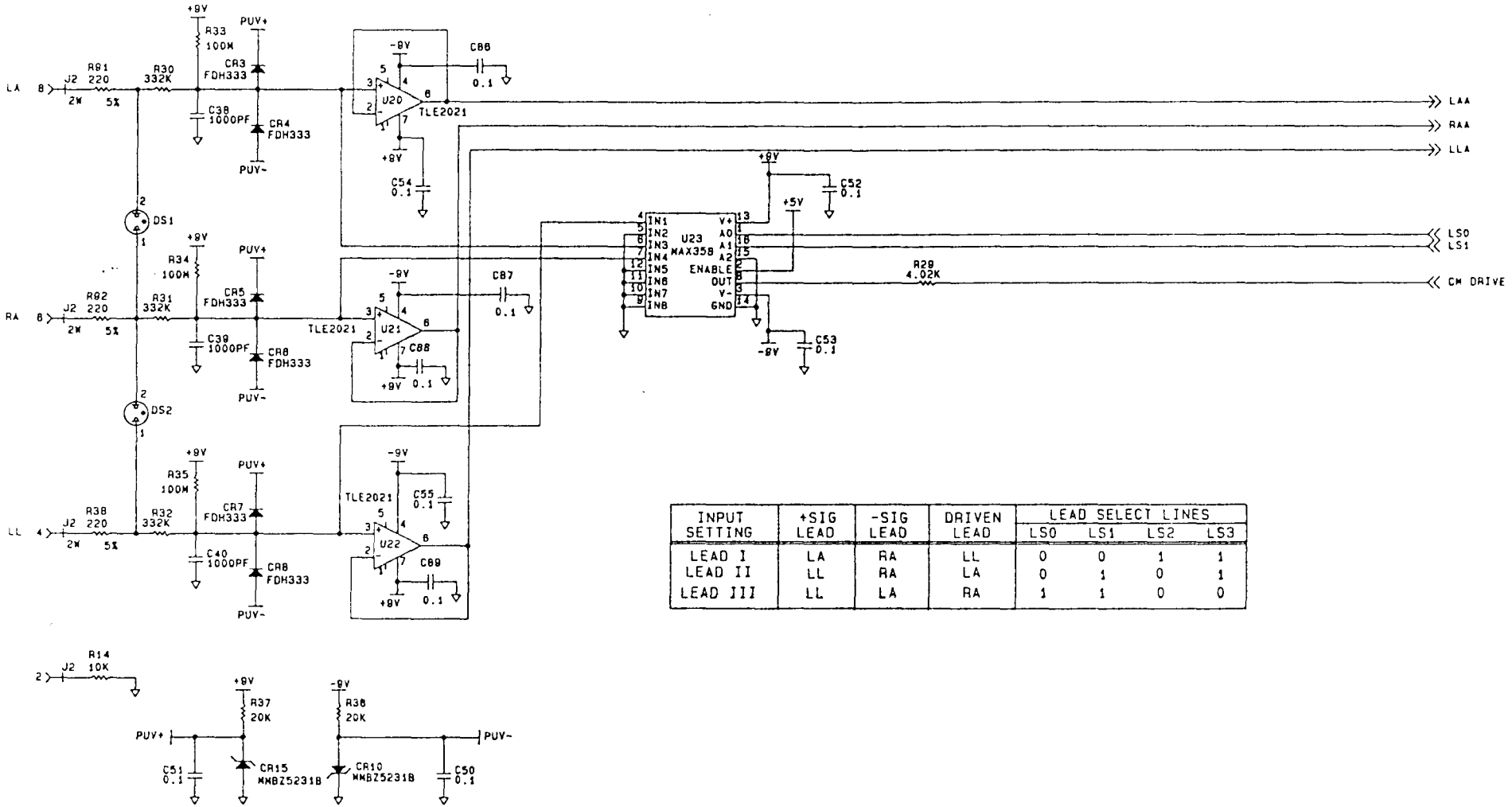
NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTOR VALUES ARE IN OHMS, +/-1%
   B. CAPACTOR VALUES ARE IN MICROFARADS, +/-10%

SC315-370 PD
DAS Board Schematic (1 of 5)

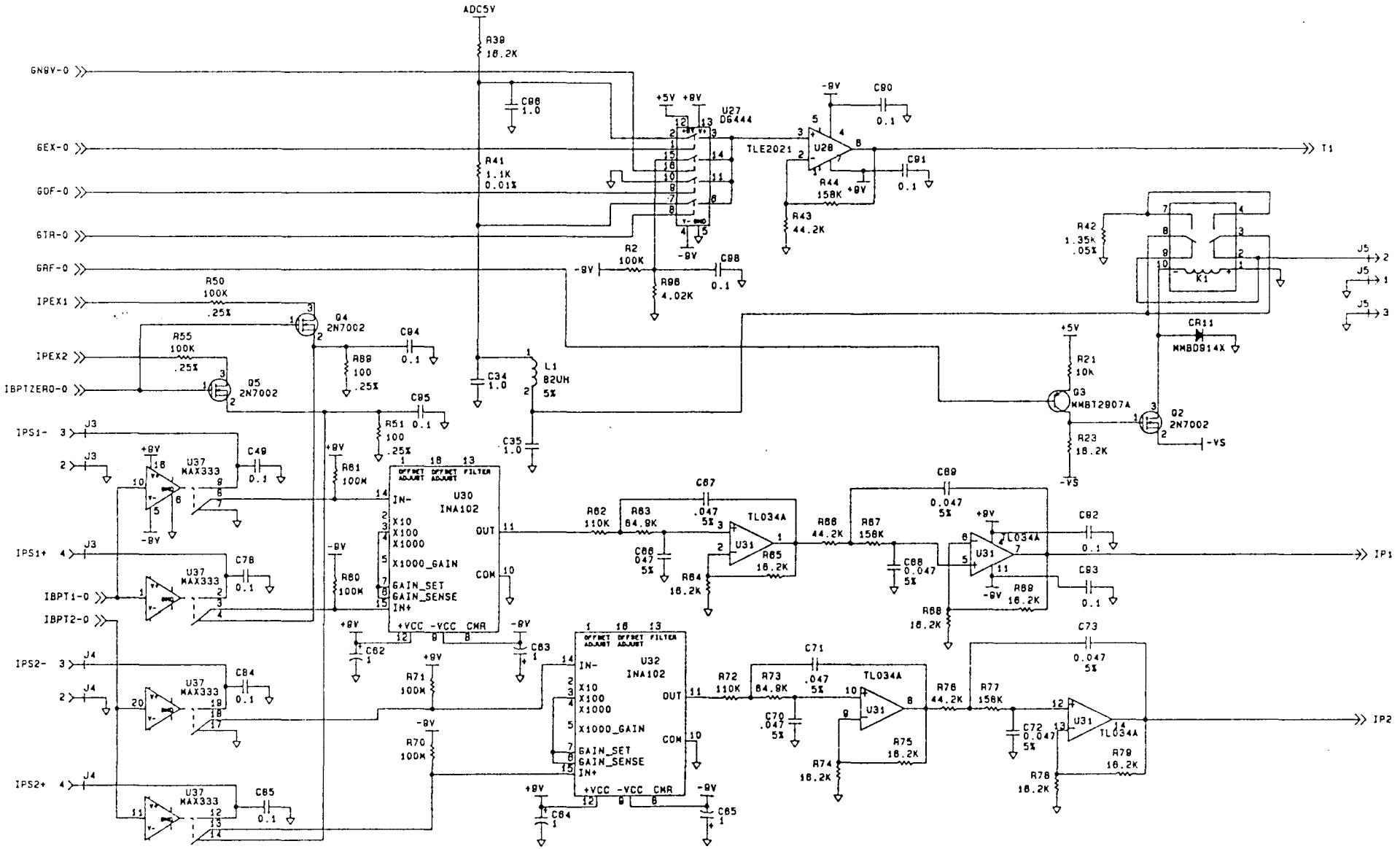


SC315-370 PD
DAS Board Schematic (2 of 5)

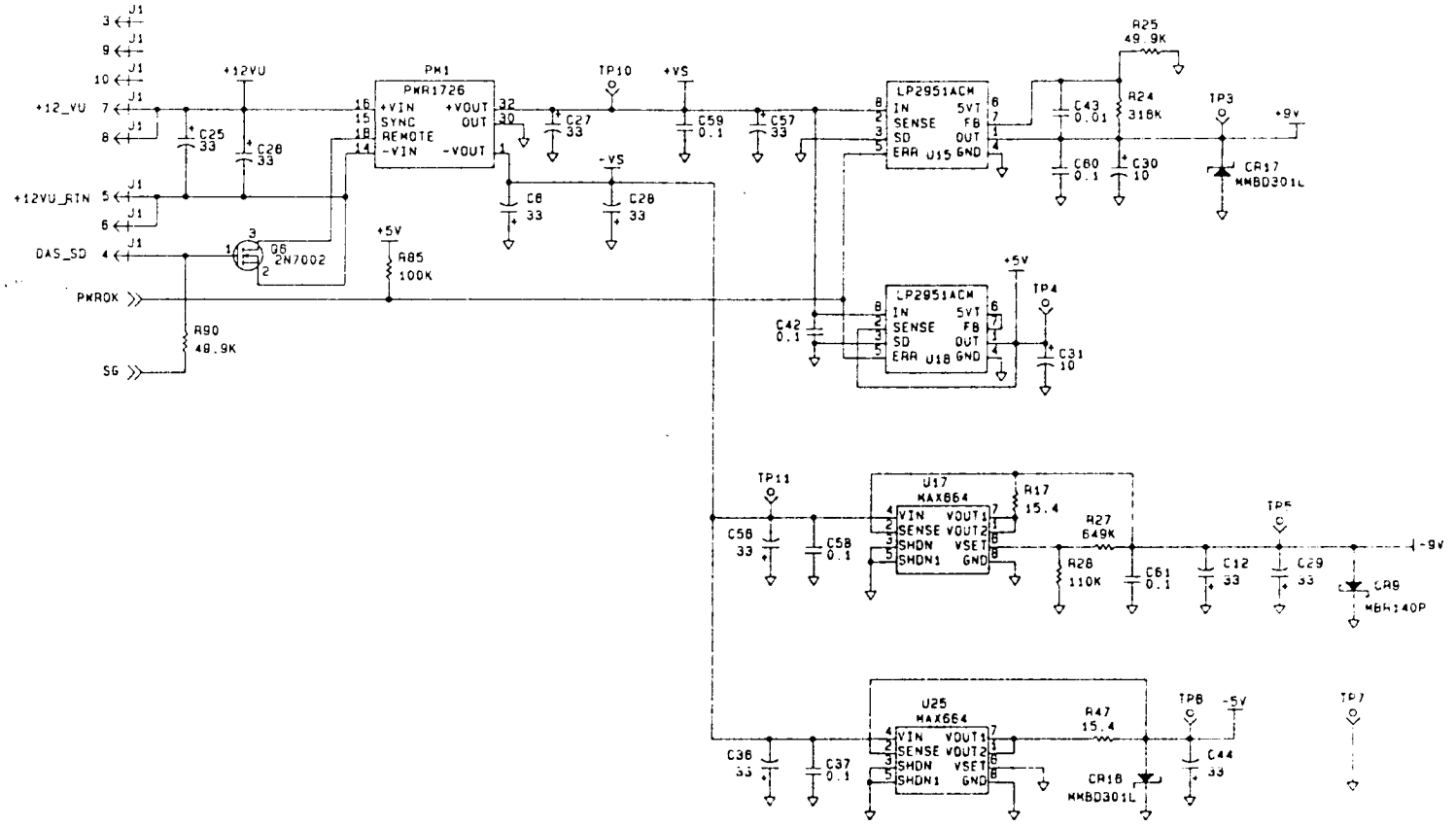


INPUT SETTING	+SIG LEAD	-SIG LEAD	DRIVEN LEAD	LEAD SELECT LINES			
				LS0	LS1	LS2	LS3
LEAD I	LA	RA	LL	0	0	1	1
LEAD II	LL	RA	LA	0	1	0	1
LEAD III	LL	LA	RA	1	1	0	0

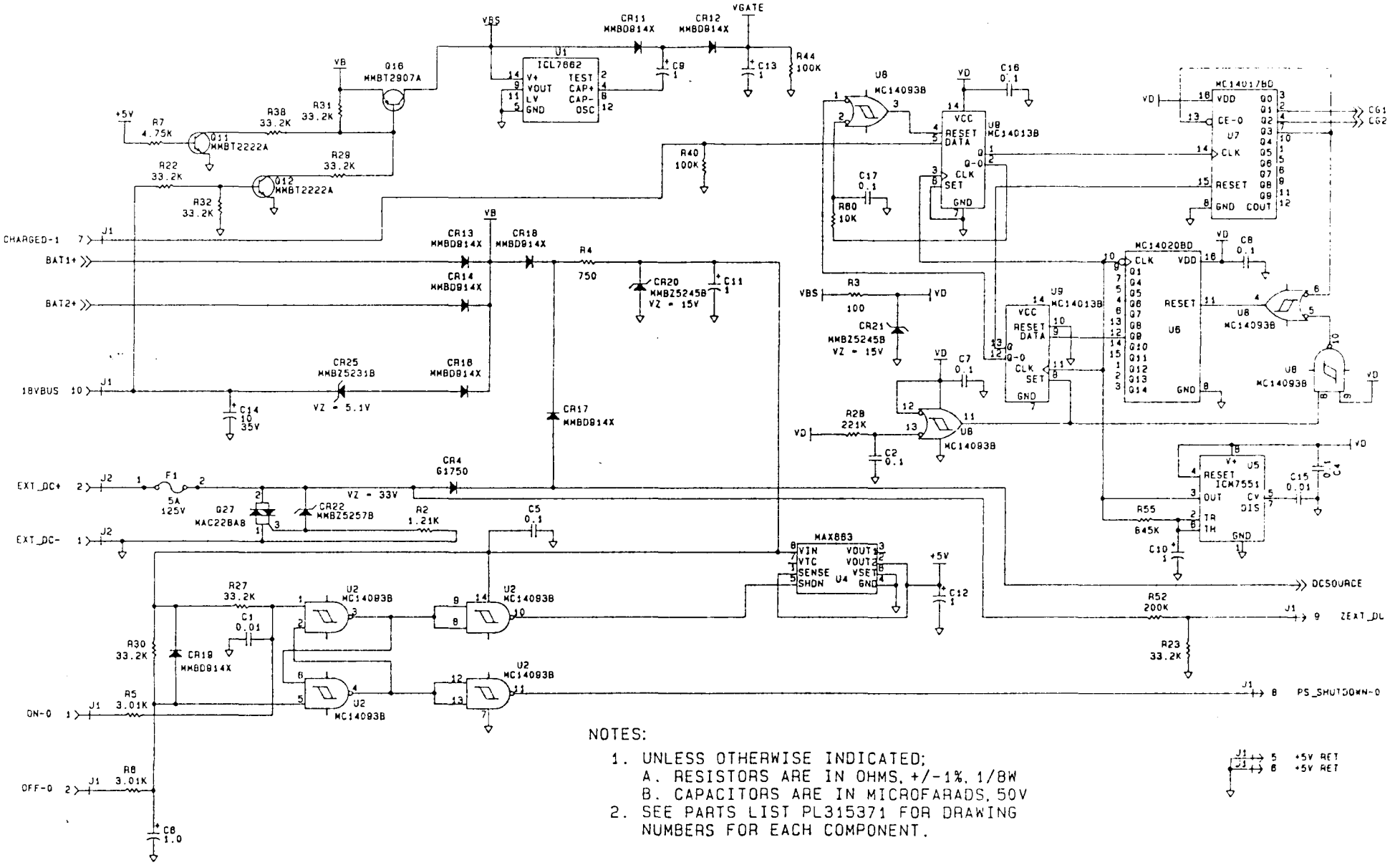
SC315-370 PD
DAS Board Schematic (3 of 5)



SC315-370 PD
DAS Board Schematic (4 of 5)



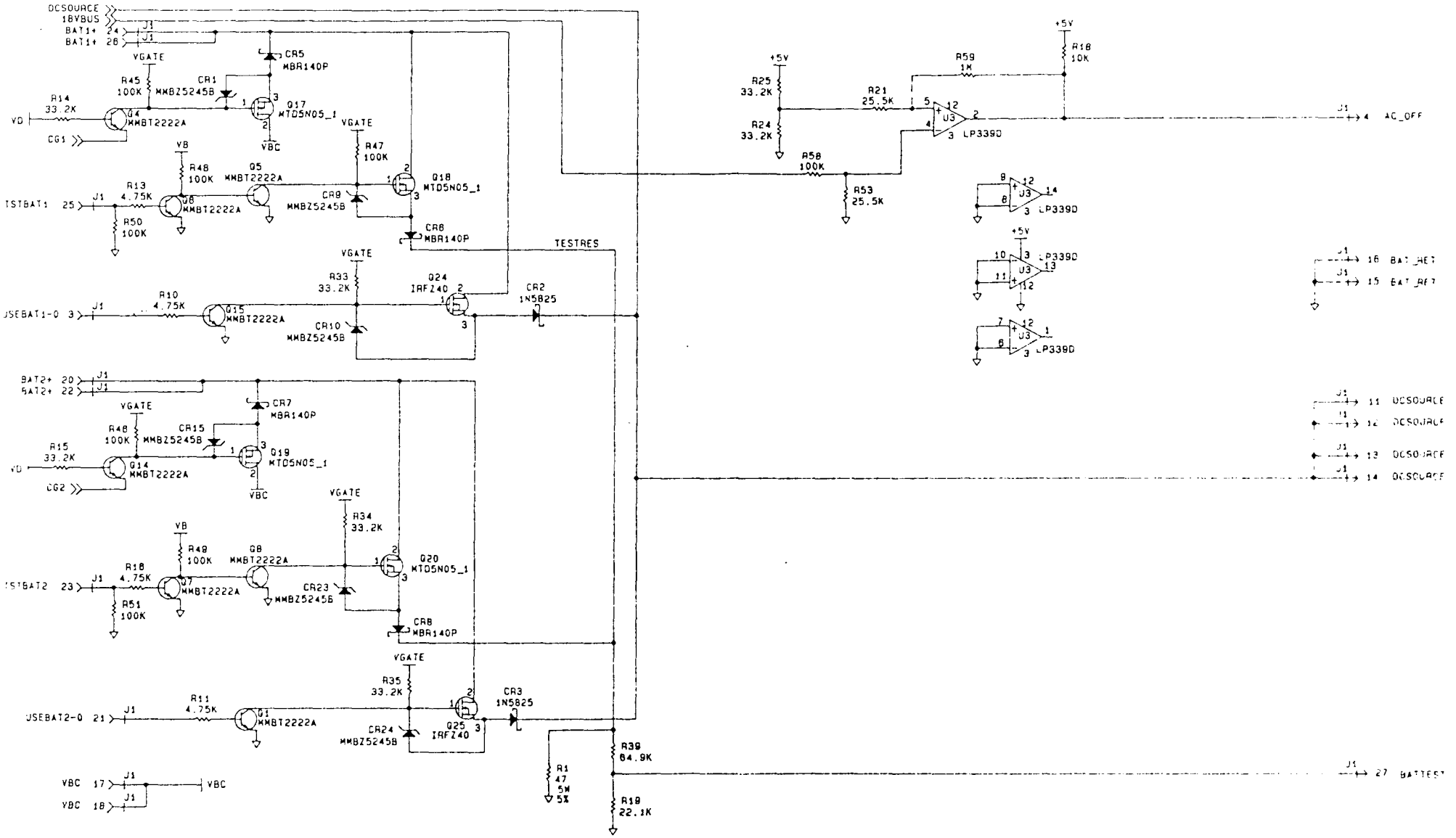
SC315-370 PD
DAS Board Schematic (5 of 5)



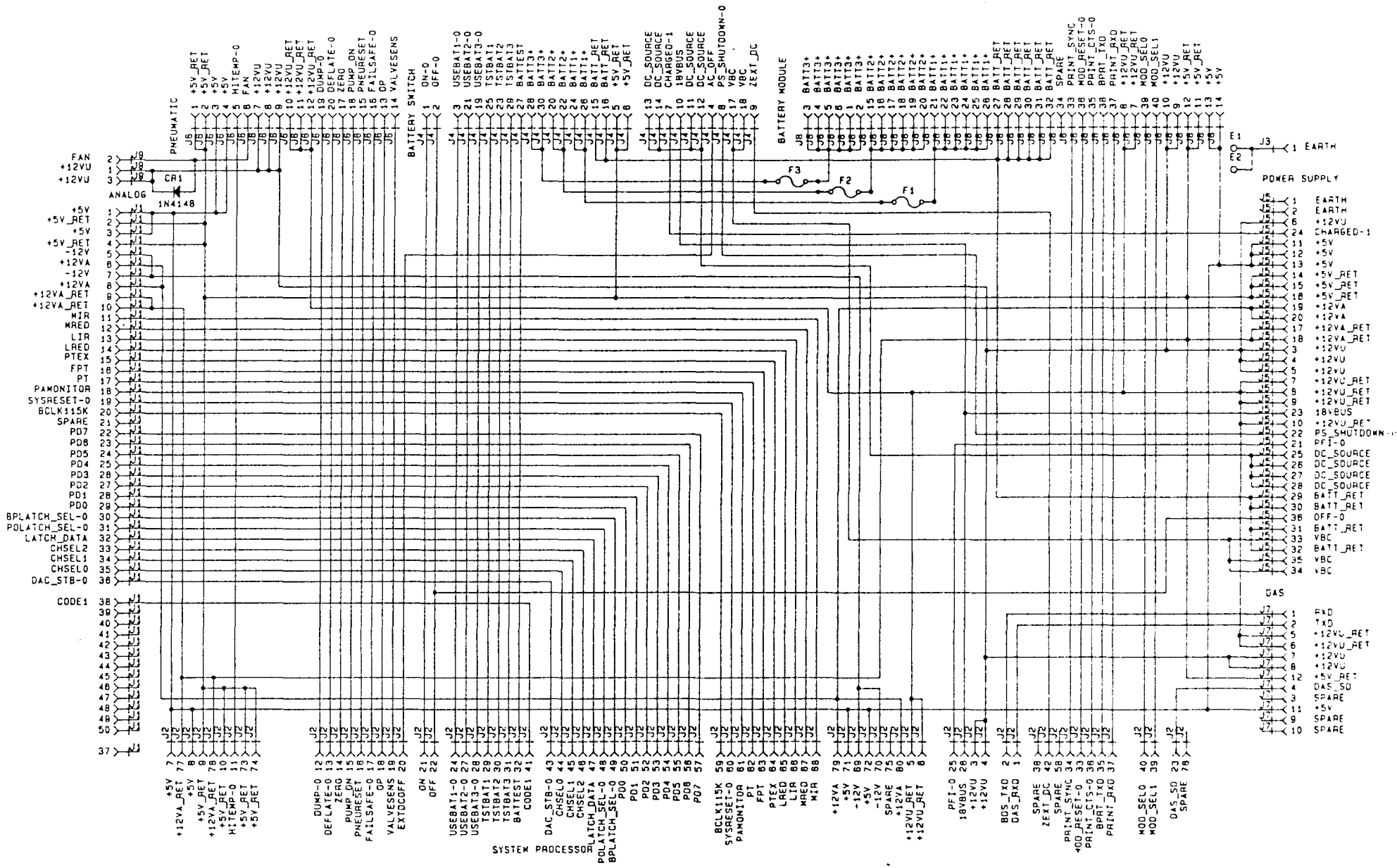
NOTES:

1. UNLESS OTHERWISE INDICATED;
   A. RESISTORS ARE IN OHMS, +/-1%, 1/8W
   B. CAPACITORS ARE IN MICROFARADS, 50V
2. SEE PARTS LIST PL315371 FOR DRAWING NUMBERS FOR EACH COMPONENT.

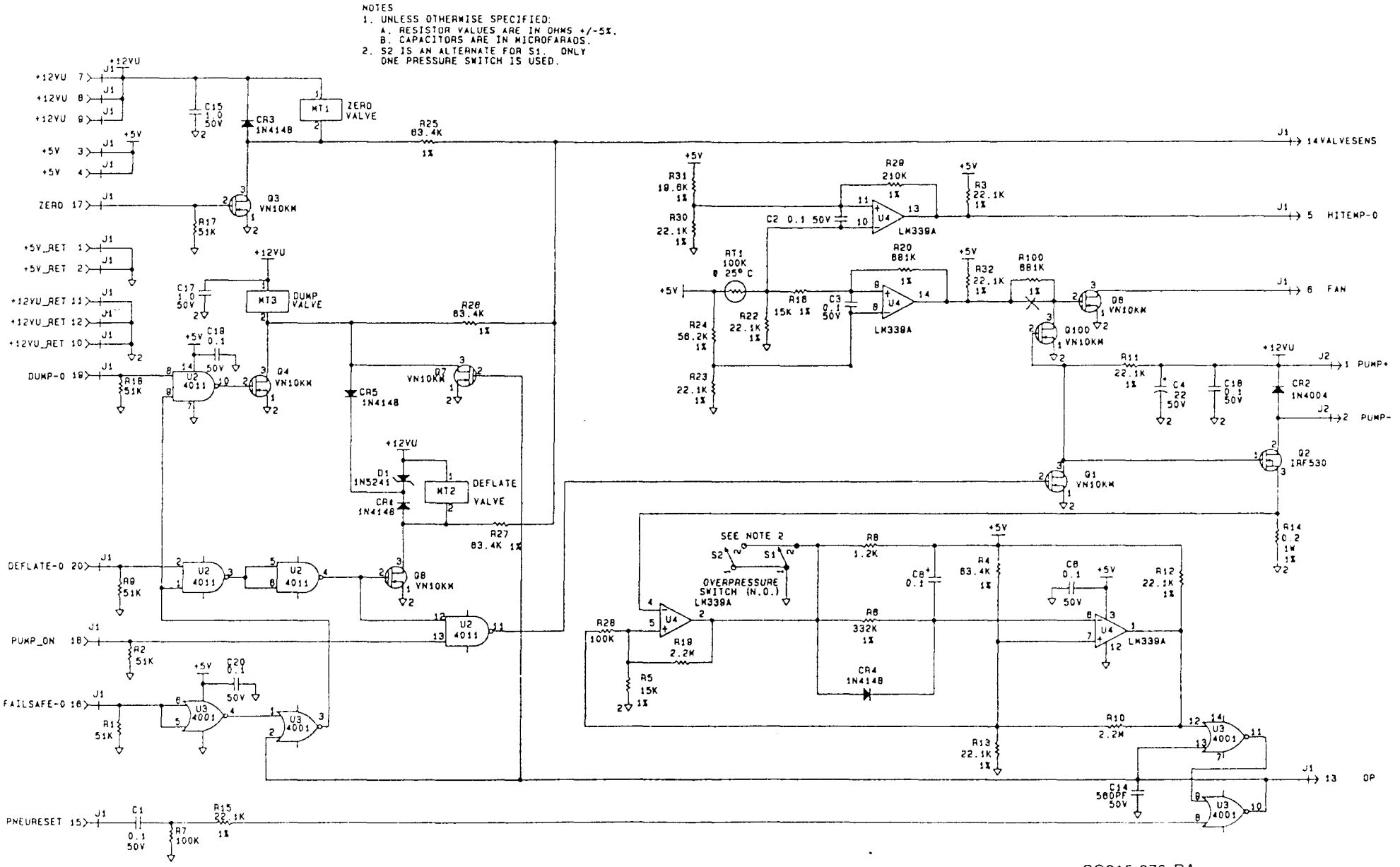
SC315-371 PB
Battery Switch Board Schematic (1 of 2)



SC315-371 PB
Battery Switch Board Schematic (2 of 2)



SC315-373 PA
Motherboard Schematic (1 of 1)



SC315-376 PA
Pneumatics Board Schematic (1 of 1)